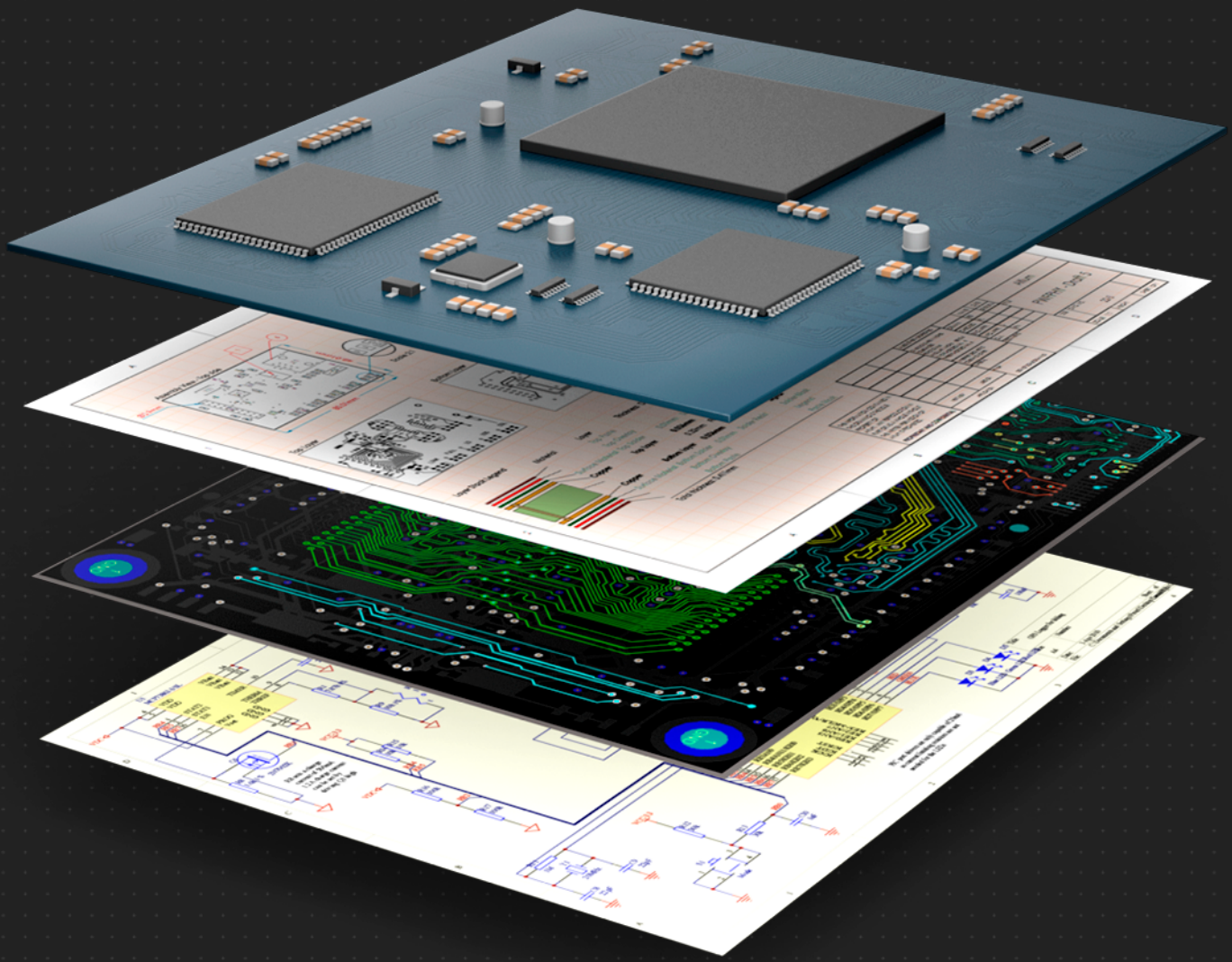
Altium

Design for Manufacturing



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Design for Manufacturing

A Practical Guide for "Right the First Time" PCB Design and Manufacturing

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The Age of Information

I've been in the electronics industry for more than 17 years, and have made a ton of mistakes along the way. But in this digital age that we all live in, information is only a search away, and the design problems that used to plague electrical engineers in the past have largely been ironed out by someone, somewhere. Never before in PCB design has information been so readily available, and problems documented so thoroughly. How does this affect you as an electronics designer? There is no need to continue re-inventing the wheel and making the same cycle of mistakes as our predecessors did in years past.

Whether I talk to seasoned electrical engineers or those fresh out of university, I'm always asked the same question - how do I design better? We are all dealing with the complexities of denser boards, higher clock rates, and smaller mechanical enclosures, and designing for those requirements alone can be a challenge. However, your designs exist beyond the digital domain, and to successfully produce a manufacturable board there are a number of additional guidelines to carefully consider throughout your entire design process.

The reality is, the process of designing better doesn't end the minute you ship off your documentation to manufacturing, it ends when you get your board back in its physical form and it works as intended. This goal can be a challenge for most PCB designers, who commonly have to deal with a myriad of unique requirements that each manufacturer sets forth, only to get lost in the details as design projects run off their intended course.

Here's the good news - there's a way to design your PCB not just for the digital domain, but for the manufacturing world as well. And when you design it correctly, you will start seeing your boards get back right the first time.

You can think of this guidebook as an accumulation of knowledge that has been set down from those before you. The collective years of experience in the electronics industry have allowed us at Altium to soak up knowledge from PCB designers all around the world, and this knowledge we now pass on to you.

Would you like more information? Watch our webinar on DFM Tips and Tricks.

Samuel P. Sattel, Director of Technical Marketing

What is Design for Manufacturing?

The goal for this guidebook is simple - get a good board back, every time. And the applied methodology for doing this is Design for Manufacturing (DFM). You might have heard of DFM in the past, but what exactly does it mean?

> *Design for Manufacturing (DFM) is the process of designing a PCB that is both manufacturable, functional, and reliable.*

With this definition in mind, we have several clear goals to reach by adopting the design practices within this guidebook:

1. Eliminate the need for multiple board respins due to manufacturing-specific details that were missed in a design process.
2. Design and produce boards that are both manufacturable and function as intended by following a set of best practices set forth by PCB design veterans.
3. Reduce the time spent on design revisions and ultimately meet time to market goals consistently by following a set of best practices for board layout and documentation

To meet these goals, we've structured this guidebook to ideally be read from start to finish to match up with your design workflow. As you read each section in the following chapters you will be able to apply the knowledge to each stage of your PCB design process.

What You Will Find in This Guidebook

This guidebook is both theoretical and practical, and applies trusted and accepted design science that has resulted in consistently manufacturable boards. The major sections in this guidebook includes:

Section 1: Design Guidelines for Successful Manufacturing

In this section we will be covering design practices that will produce both a functional and manufacturable board layout. This section will include:

- **Chapter 1:** Understanding the typical PCB manufacturing process and its various stages.

- **Chapter 2:** Selecting the right materials for your PCB to meet your specific design requirements.
- **Chapter 3:** Strategizing your PCB layout including via/hole placement, soldermask layers, and silkscreen documentation.
- **Chapter 4:** Placing and orienting your components to ensure proper spacing and assembly.
- **Chapter 5:** Configuring test point requirements for successful board testing by your manufacturer.

Section 2: Documentation Guidelines for Successful Fabrication and Assembly

With your design complete and ready for manufacturing, we will then be moving on to properly documenting a PCB to provide crystal-clear design intent to your manufacturer. This section will include:

- **Chapter 6:** Understanding what the main factors are in the PCB documentation process and what needs to be sent to your manufacturer.
- **Chapter 7:** Assembling the master drawing of your PCB to accurately portray all of the fine details needed to manufacture a board.
- **Chapter 8:** Understanding what you need to include in your assembly documentation to have your bare board created with your selected components.
- **Chapter 9:** Understanding why manufacturing files matter and what specific files to send to your manufacturer including Gerbers, ODB++, IPC-2581 and Bill of Materials.

By the end of this guidebook you will be well equipped to implement the design and documentation practices into your own personal workflow to produce manufacturable-ready PCBs.

Design Guidelines for Successful Manufacturing

A Day in the Life of a PCB Manufacturing Process

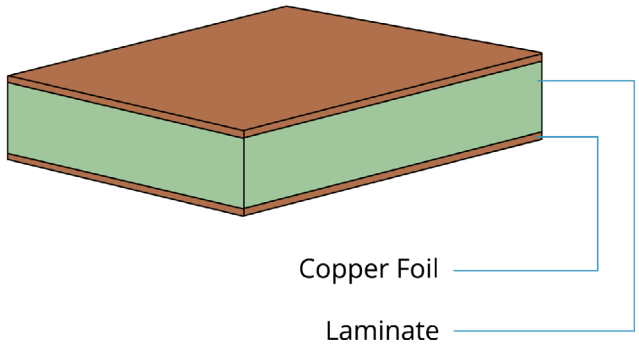
Before undertaking a Design for Manufacturing process, it is important to understand the underlying process behind producing a physical PCB. Regardless of the various technologies present in each facility, a large majority of industry-leading manufacturers follow a specific set of steps to turn your design from digital bits to physical boards. The steps in this process are outlined in Figure 1 and includes:

Standard PCB Manufacturing Process

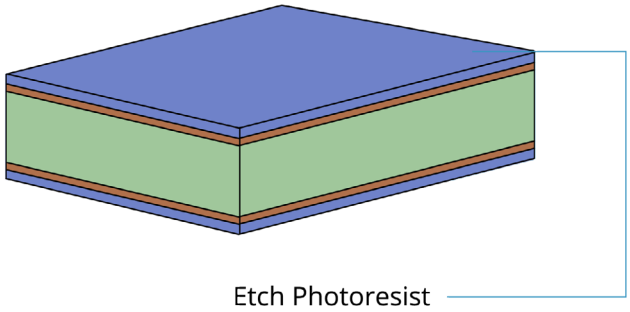
Data Transfer from Customer: Gerber, GerberX2, IPC-2581, ODB++, Netlist, NC-Drill, Fab Drawing, Specs

Data Prep: Conversion of customer supplied data to tooling (Panelization, Artwork, Drill and Route programs)

Cores/Laminate: Thin laminate material consisting of glass epoxy substrate clad with copper on sides (FR-4 is most commonly used material for PCB design)



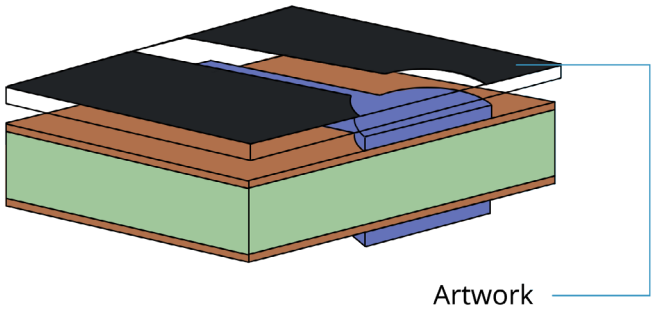
Dry Film Resist Coating: Using heat and pressure, a light sensitive film is applied to the copper surface of the core.



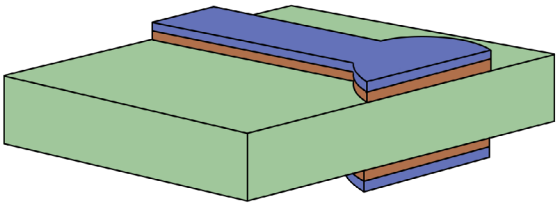
Place Artwork: Artwork patterns from the customer (circuits and land patterns) are placed on the film coated surfaces of the core. Each surface has its own artwork pattern.

Expose Panels to Ultraviolet Light: This creates a latent image of the circuit board.

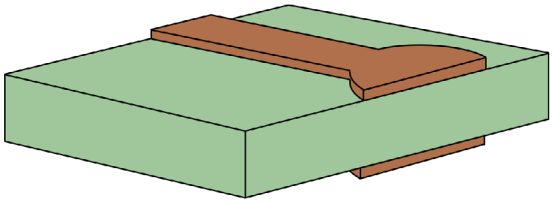
Develop Panels (resist removal): Chemically remove the resist from areas not hardened by passing the exposed core through a chemical solution.



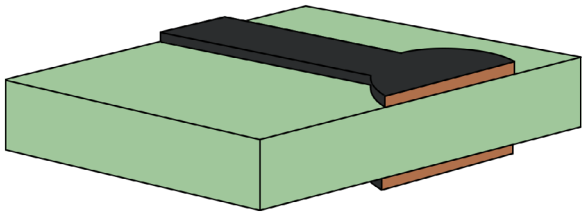
Etch: To chemically remove copper from core in all areas not covered by film resist, which creates a discrete copper pattern.



Strip Resist: Chemically remove the developed dry film resist.

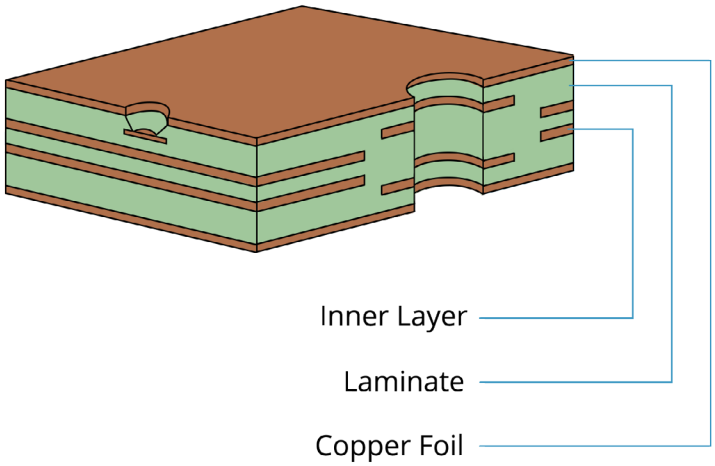


Oxide Coating: Chemically treat copper to roughen surface and improve adhesion to prepreg during the lamination cycle.



Multilayer Lamination: Copper foil, prepreg (multilayer glue), and cores are bonded together under heat and pressure.

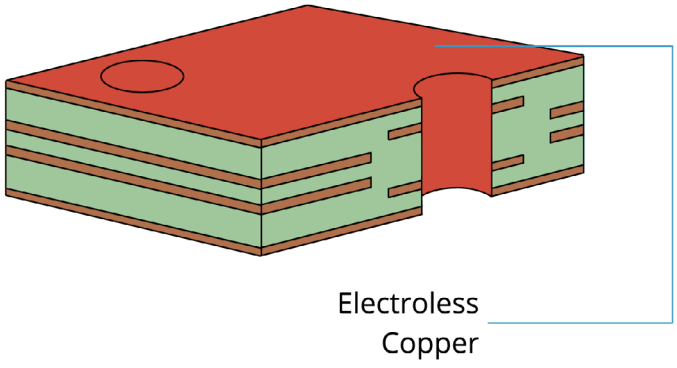
Primary Drilling: Holes are drilled through a stack of panels (double sided/single sided start here).



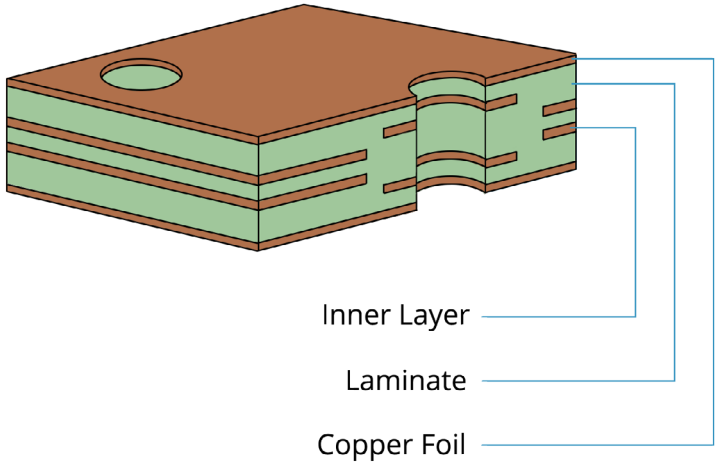
Deburr and Clean: Mechanically remove copper burrs and clean debris from drill holes.

Desmear: Chemically remove resin coating from the hole wall.

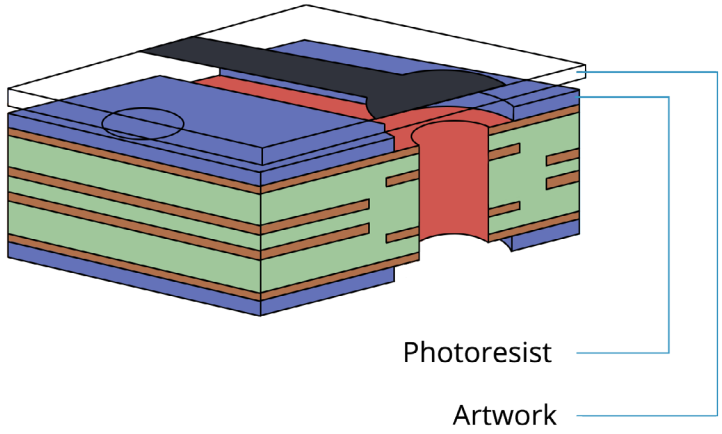
Copper Deposition: Chemically deposit a thin coat on the panel surface and hole walls.



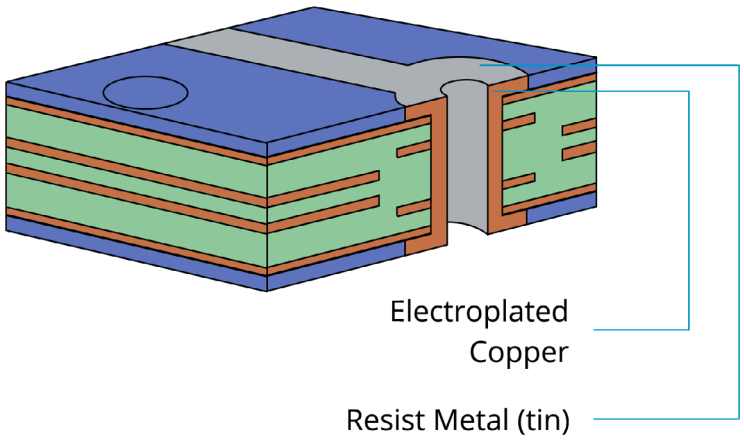
Dry Film Photoresist Coat: Using heat and pressure, a light sensitive film is applied to the copper surface.



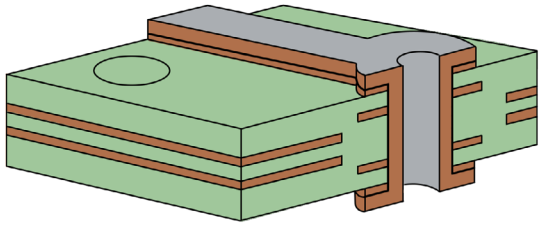
Expose & Develop: Similar to the inner layer process for the core.



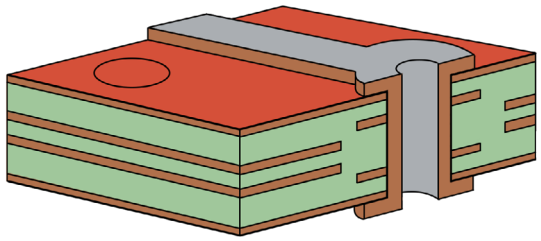
Copper Pattern Plate (electroplating): Additional copper (as well as tin) is electrically plated into the exposed electroless copper surfaces, as well as tin.



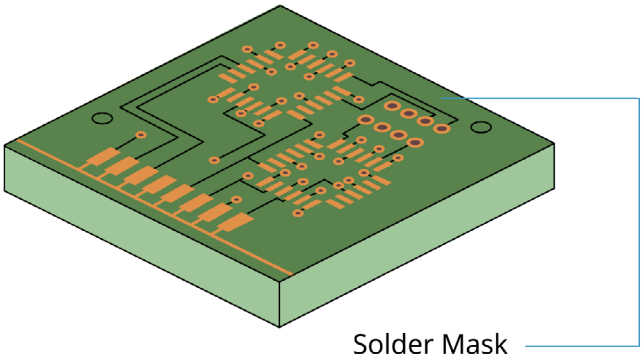
Etch: Copper is now removed from any area not covered by tin.



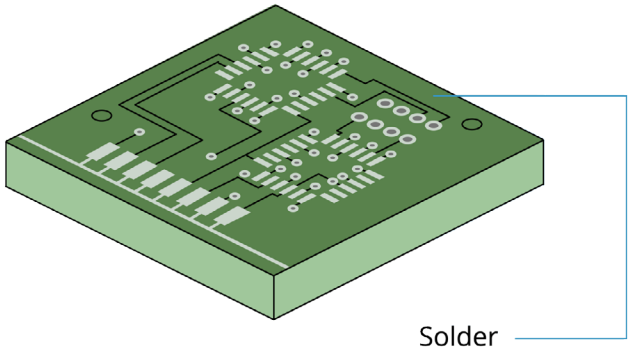
Strip Resist: Developed dry film resist is chemically removed. Tents that were placed have prevented plating from occurring in “non-plated” holes.



Solder Mask and Cure: Liquid photoimageable mask is applied to each surface and dried to the touch. Artwork is also applied and exposed. PPanel is developed, leaving mask pattern defined by artwork.



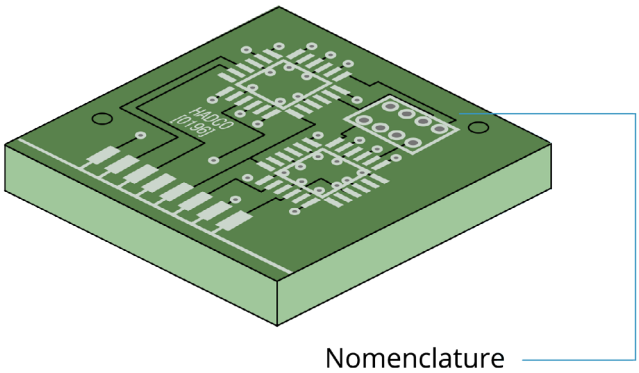
Hot Air Solder Leveling (most common PCB surface finish): Panels processed through a molten solder bath, which covers all exposed copper surfaces.



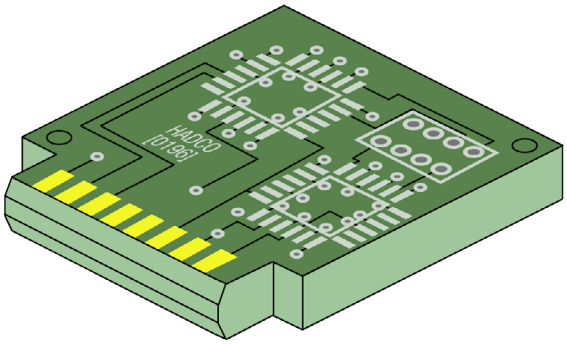
Surface Finishes: RoHS or not RoHS compliant.

Hot Air Leveling (HAL, HASL): Convey PCB through flux station, solder bath, and then through air knives (to remove level excess solder).

Legend and Cure: Top and bottom overlays (silkscreens) are inked onto each side of the panel per customer artwork, then the panels are baked to cure the ink.



Fabrication and Routing: Board is cut to size (a.k.a routing, scoring, punching, or profiling). Slots and chamfers are also added during this step.



Electrical Test/Final inspection: Board is tested for electrical integrity (and impedance if required). Shorts and opens are repaired at this point. Flying probes are usually used for smaller lots, and bed of nails test fixtures are used for larger volumes. Other functions usually performed during this step include: automatic optical inspection (AOI) which compares the inner and outer layers cost drivers on PCB against downloaded CAM data for integrity and design rules, reliability testing, and statistical process control (SPC) when required by the customers.

With the final curing of your board complete, a manufacturer will then begin the electrical test process with the provided test points you established on your board layout. All boards that pass this verification process are considered complete and then make their way through shipping and transport.

Typical Cost Drivers in the PCB Manufacturing Process[1-1]

The cost to have your board manufactured is largely determined by the specific materials and parts that you specify during your design phase. Informed engineers will take their time to carefully balance cost drivers with the need to meet intended functional requirements as outlined in their product's specifications. Some of the most common cost drivers and cost reduction strategies in the manufacturing process are outlined in the table below and includes:

Cost Driver	How to Reduce It
PCB size, shape and edge clearance	Panelize and add tabs
Non-standard parts and packaging	Use standard parts and packaging
Layer counts	Reduce the number of layers if possible
Build/Complexity	Reduce complexity (buried vias, etc...)
Additional manual setups	Place components on one side of board
Number of part types	Minimize component types used
Parts placed manually	Use press-fit or SMDs
Selective solder fixtures	Use press-fit or single sided SMD
Component pre-load capability	Component lead design allows pre-loading
Hole size and quantity	Reduce and use standard hole sizes
Two-sided assembly	Use captive press-fit studs

Making Manufacturing-conscious Design Decisions

By understanding the above knowledge about the typical PCB manufacturing process, you will be well on your way towards making more informed choices at design time for materials and part selections. With an understanding of the manufacturing process behind us, it is now time to jump into a practical Design for Manufacturing process, starting with material selection.

Selecting Your Materials

Introduction

Every design process begins with material selection, and this chapter focuses on selecting the right materials for your PCB design given the particular design requirements you outline in your specifications. We will be focusing largely on FR-4 as it is the most commonly used material for PCB design. If your specific material requirements are not listed in the sections below, please contact your manufacturer for further guidance.

Basic Material Selection Process

When designing a PCB, there are several material choices to consider based on your unique design needs. Before selecting a material, it is recommended to first define the functionality and reliability requirements that your board must meet. These requirements will typically include:

- Electrical properties
- Thermal properties
- Interconnections (soldered components, connectors, etc...)
- Structural board integrity
- Circuit density

As a general rule, remember that the more you increase your design complexity and properties the more costs you will incur during your manufacturing process. A carefully crafted balance should always be made to meet both budget, functionality, and reliability goals for your particular design needs. See Figure 2 for a visual on how to begin your material selection process[2-1].

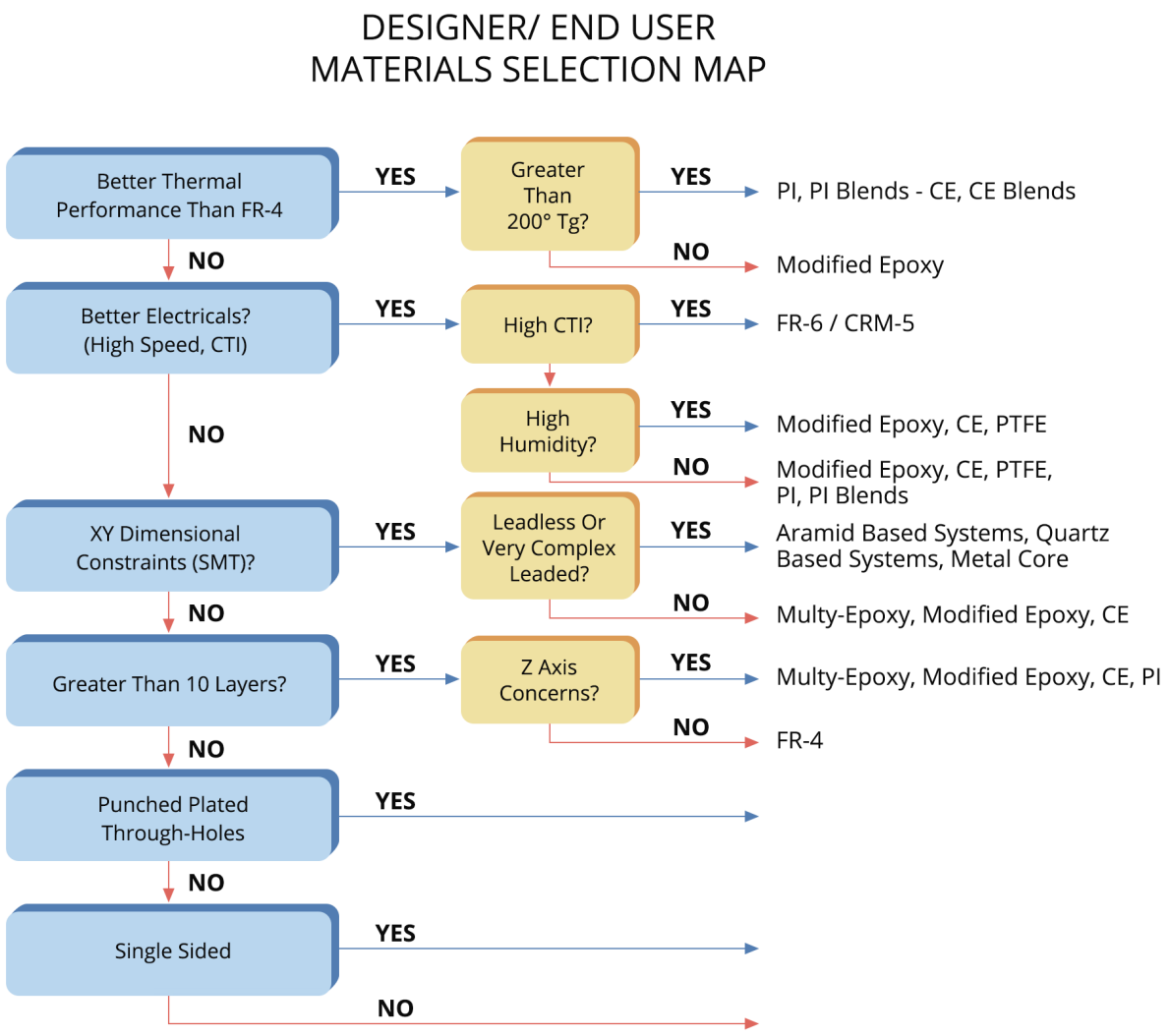


Figure 2 - Designer/End-User Materials Selection Map[2-1]

Additional Criteria for Material Selections

As you begin constructing a composite from your chosen materials, you will want to pay close attention to temperature characteristics. In practice, the lowest-rated material will dictate the maximum end product temperature. Other items that should also be considered when comparing different materials includes:

- Resin formula
- Flame resistance
- Thermal stability
- Structural strength
- Electrical properties
- Flexural strength
- Maximum continuous safe operating temperature
- Glass transition temperature (Tg)
- Reinforcing sheet material

- Nonstandard sizes and tolerances
- Machinability or punchability
- Coefficients of thermal xpansion (CTE)
- Dimensional stability
- Overall thickness tolerances

The sections that follow will dive into some of the various material properties in detail for the primary components that make up a PCB design including electrical properties, FR-4, and copper.

Material Properties in Detail

Electrical Properties

The most critical properties to consider for electrical requirements are the electrical strength, dielectric constant, and moisture resistance.
Refer to Figure 3 for a list of some of the more common materials and their associated property values. Remember to consult with your manufacturer for more specific data on electrical properties.

Property	Material					
	FR-4 (Epoxy E-glass)	Multifunctional Epoxy	High Perfomance Epoxy	Bismalaimide Triazine/Epoxy	Polyimide	Cyanate Ester
Dielectric Constant (neat resin)	3.9	3.5	3.4	2.9	3.5-3.7	2.8
Dielectric Constant (reinforcement)	—	—	—	—	—	—
Electric Strength (V/mm)	39.4×10^3	51.2×10^3	70.9×10^3	47.2×10^3	70.9×10^3	65×10^3
Volume Resistivity (D-cm)	4.0×10^6	3.8×10^6	4.9×10^6	4×10^6	2.1×10^6	1.0×10^6
Water Absorption (wt%)	1.3	0.1	0.3	1.3	0.5	0.8
Dissipation Factor (DX)	0.022	0.019	0.012	0.015	0.01	0.004

Figure 3 - Typical Properties of Common Dielectric Materials [2-2]

FR-4 Default Values

The default values in Figure 4 below for FR-4 can be used as a baseline for determining your specific material requirements. These values will change depending on your specified base material and thickness as shown in the next sections.

		FR4 Standart	FR4 High-TG	FR4 Halogen Free	FR4 KF	Polyimid
TG	˚C	> 135	>170	>140	>135	>230
CTE-z	ppm/˚C	60	45	45	50	20
Permittivity εr	bei 1MHz	4.6	4.8	4.7	4.7	3.4
Electrical strength	KV/mm	45	55	50	45	125
Surface resistivity	MΩ	10^6	10^7	10^7	10^7	10^6
Tracking resistance CTI	V	PLC3*	PLC3*	PLC3*	PLC1 / PLC**	—
Td value	˚C	301	345	360	310	***
Peel strength	N/mm	1.1-1.6	1.2	1.4	1.6	1.6
Flammability class	UL-94	V0	V0	V0	V0	V0
Standart		IPC-4101	IPC-4101	IPC-4101		IPC-4204

Figure 4 - Default FR-4 Material Values[2-3]

FR-4 Base Material and Thickness

The values in Figure 5 below list the most common FR-4 materials used today for multilayer board designs and will help you to choose the appropriate thickness for your FR-4. The thickness of specific variations of FR-4 including GETEK®, Rogers®, FR-406 and FR-408 are similar and can also be calculated using this table.

Core	Coper Weight (oz)	Nominal Material Thickness (mm)	Measure Material Thickness (mm)
(Basic material with copper)		(Base material)	
5	0.5/0.5	0.125+0.025	0.125
6	0.5/0.5	0.150+0.025	0.142
8	0.5/0.5	0.200+0.025	0.188
10	0.5/0.5	0.250+0.038	0.228
12	0.5/0.5	0.300+0.038	0.227
15	0.5/0.5	0.380+0.05	0.358
21	0.5/0.5	0.635+0.0635	0.632
28	0.5/0.5	0.711+0.0635	0.716
42	1/1	1.066+0.125	1.069

Figure 5 - FR-4 Material Thickness Reference[2-4]

FR-4 Prepreg Designation and Thickness

Prepreg (Pre-impregnated) is the sheet material (e.g. glass fabric) that is cured with a resin and cured to an intermediate stage. Most PCB manufacturers will carry five types of prepreg including 106, 1080, 2113, 2116, and 7628. Refer to Figure 6 for specific thickness specifications for each prepreg type.

> *Note: There are limitations to the type and number of prepreg sheets that can be placed between board layers. Consult with your manufacturer about your specific board layout needs to determine your correct prepreg designation and thickness.*

Glass Style	Glass Style Thickness mm
106	0.053 (0.002”)
1080	0.0787 (0.003”)
2113	0.100 (0.004”)
2116	0.135 (0.005”)
7628	0.193 (0.0075”)

Glass Style	Resin Content	Thickness* (Mils)
106	72-77	2.1-2.8
1080	61-67	2.8-3.4
2113	53-56	3.8-4.6
2116	51-57	4.6-5.4
7628	40-46	7.2-8.0

*This is the maximum possible thickness contribution

Figure 6 - FR-4 Prepreg Designation and Thickness[2-4]

Copper Foil Types

Manufacturers will typically offer various types of foil for you to choose from, the most common being Electro-deposited Copper (ED Copper) and Rolled Copper. Rigid boards will typically use electrodeposited copper foil whereas rigid-flex boards will use rolled copper foil. Regardless of which copper foil type you choose, they will all meet your standard IPC-MF-150 requirements[2-5]. If you choose an alternative foil type such as nickel or aluminum, be sure to specify the characteristics on your master drawing to avoid any miscommunication or manufacturing issues.

Copper Resistance Values

As boards get denser and more complex, it becomes increasingly important to calculate your copper’s distributed resistance. You can use the formula[2-6] below to easily compute the resistivity in your copper traces:

R = ρ*L/A

where:

R is the end-to-end track resistance in Ohms

ρ is the resistivity of the track material in Ohm Metres

L is the track length in metres

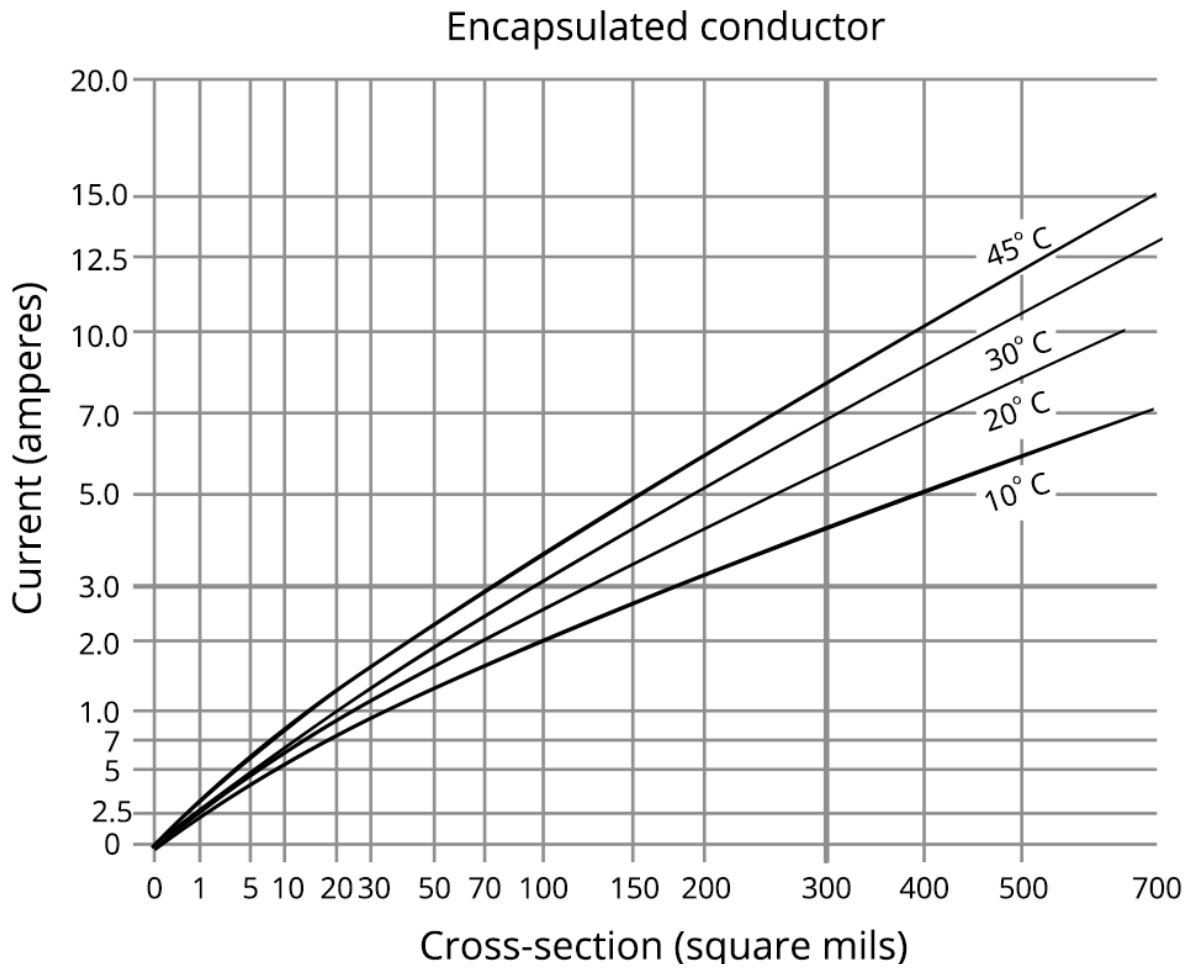
A is the track cross sectional area in square metres

You can also use one of the free tools below to quickly calculate your copper resistivity without needing to perform manual calculations:

- Circuit Calculator[2-7]
- EEWeb Trace Resistance Calculator[2-8]
- Endmemo Resistance Calculator[2-9]

Current Carrying Capacity of Copper

In Figure 7 can be used as a reference to understand the current carrying capacity of internal layers for common copper thicknesses and temperature levels above ambient. The current carrying capacity for external layers is approximately 2x that of internal layers. For more detailed data on line widths and spacing requirements refer to IPC-2221[2-10].



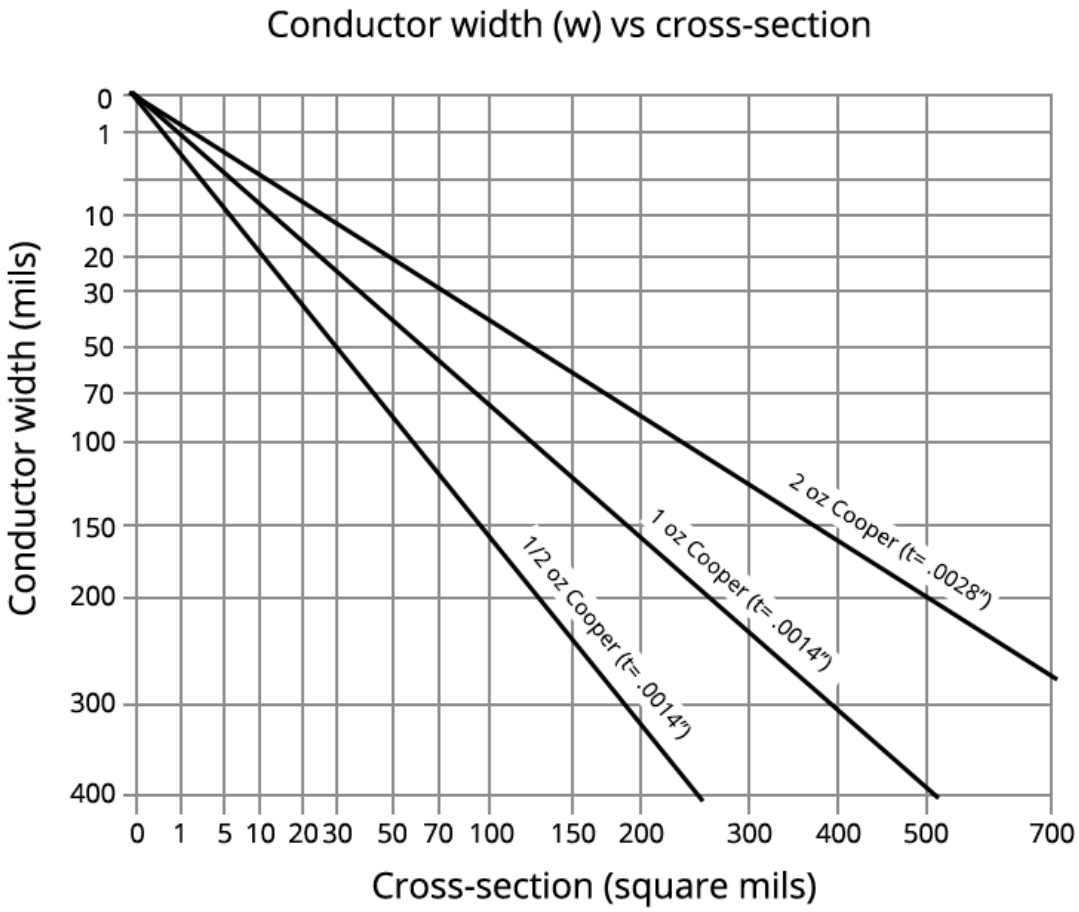


Figure 7 - Encapsulated Conductor Widths[2-10]

Finished Board Thickness

As part of your final material selection process, you will want to calculate your finished board thickness. This measurement is made from copper-to-copper and will represent your maximum finished board thickness. Some specifics to keep in mind about board thickness calculation includes:

- Board thickness will determine how your manufacturer sets up their processing machinery.
- Board thickness will affect the limitations of your board during manufacturing, including aspect ratios.
- Manufacturers typically offer lamination thicknesses between 0.0008" to 0.240" including the solder mask.
- Boards with less than 0.05" thickness will typically require special handling and processing, which could result in higher costs and longer processing times.

Finalizing Your Material Selections

You now have the knowledge needed to finalize your basic material selections for your next manufacturable-ready PCB design. To summarize, the base materials and the required property values you will need before you begin your design process includes:

FR-4	Base Material Thickness
FR-4 Prepreg	Designation Thickness
Copper Foil	Type Resistance Current Carrying Capacity

With these values in hand, you can then calculate your maximum board thickness which will have a direct impact on both manufacturing costs and processing requirements by your manufacturer. The next section will cover how to strategize your PCB layout for manufacturing including via/hole placement, soldermask layers, silkscreen documentation, and more.

Strategizing YourPCB Layout

Introduction

With your material selections finalized, it is now time to dive into the specific details of your PCB layout. While individual engineering workflows might differ from one designer to the next, there are a number of primary design considerations that have a need for precise DFM requirements to consider a board 100% ready for manufacturing. In the following sections you will learn the specifics of strategizing your PCB layout including SMT and through-hole specifications, silkscreen documentation, solder mask applications, and more.

Deciding Between Through-hole or SMT

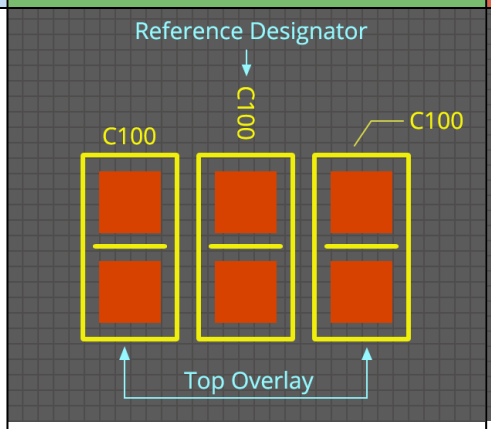
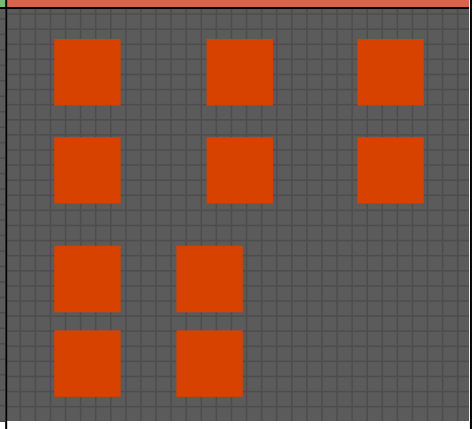
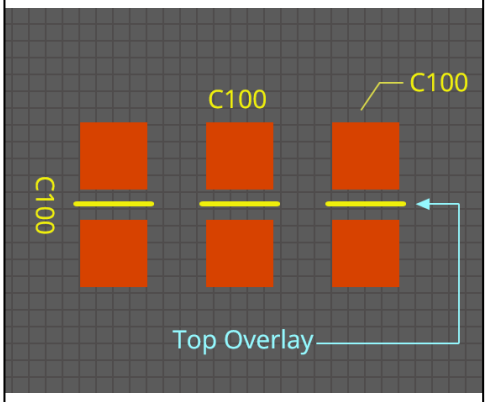
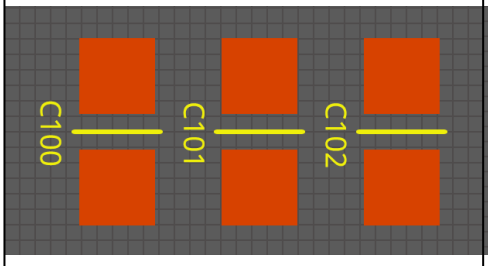
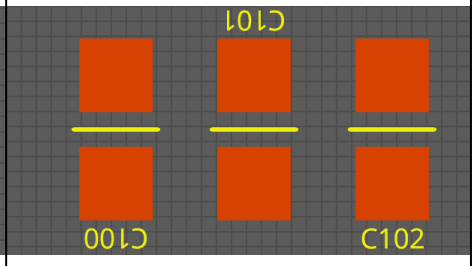
When designing a PCB, it is typical to either choose surface mount technology (SMT) or through-hole for your component applications. If you do happen to use both manufacturing methods, then your board is considered a hybrid PCB. Based on current industry trends in PCB design, it is recommended that most of your components be surface mounted devices (SMD), as this technology has dominated the PCB design market since the 1990s and includes many advantages including higher board densities at a lower cost. Keep the following in mind when deciding between SMT and through-hole:

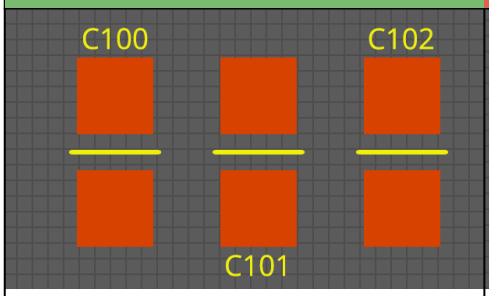
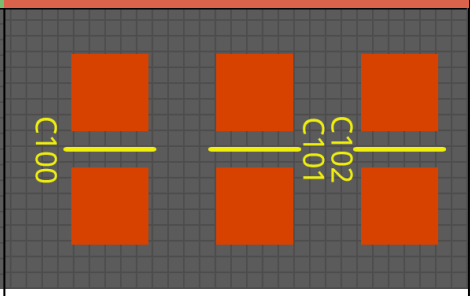
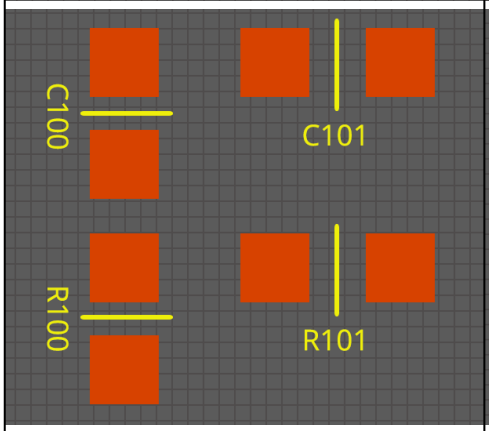
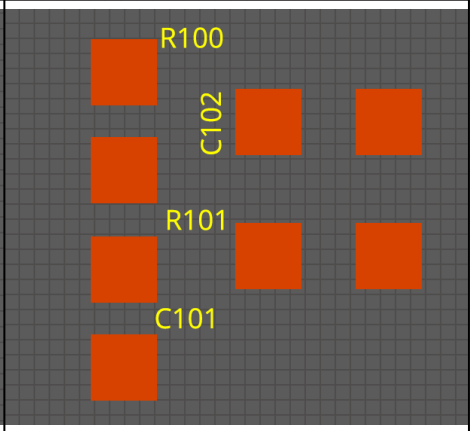
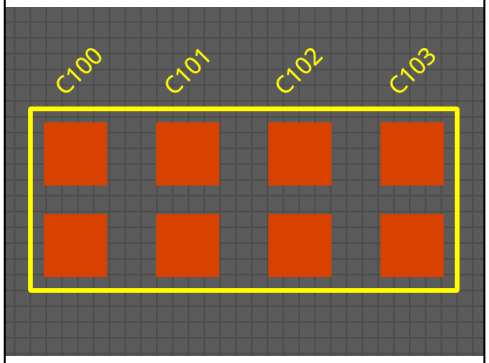
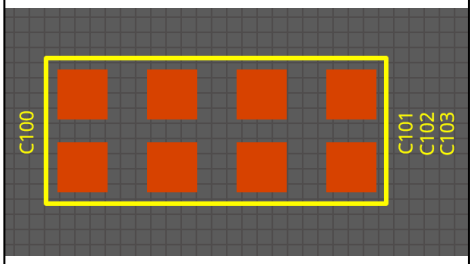
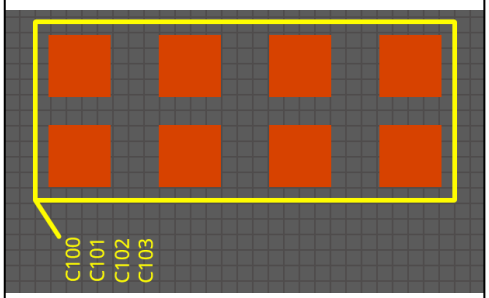
- PCBs with plated through-hole devices (PTHs) are wave-soldered, whereas PCBs with surface-mount devices (SMDs) can be wave or reflow soldered.
- Mixing these two technologies will result in separate processes to manufacture your board and will add to your overall manufacturing time and cost.
- Some manufacturers will hand-install through-hole components which will add to your overall manufacturing time and cost.

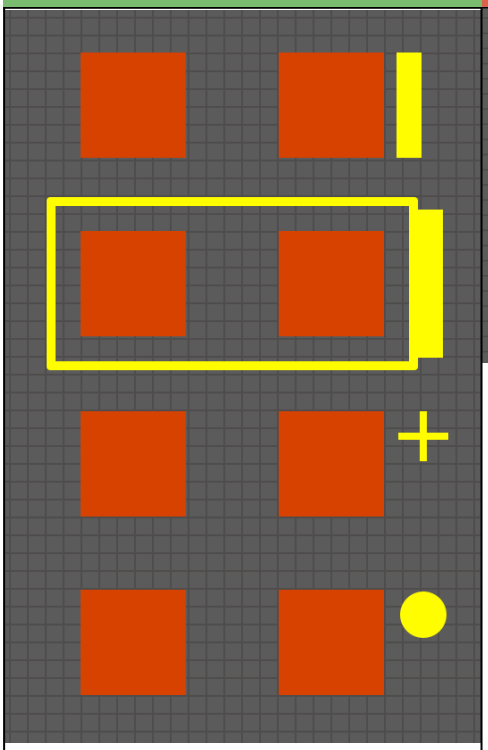
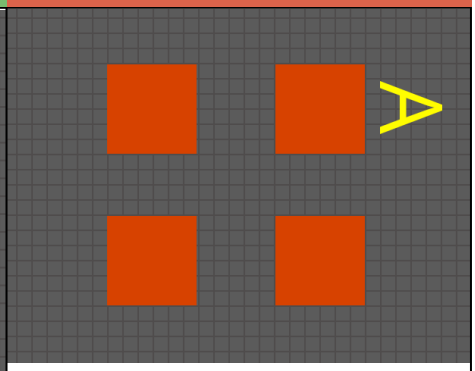
The component application method you choose will have a direct impact on your overall costs and manufacturing time. It is recommended to stick with SMT for professional board designs as this results in quicker board turnarounds and higher reliability.

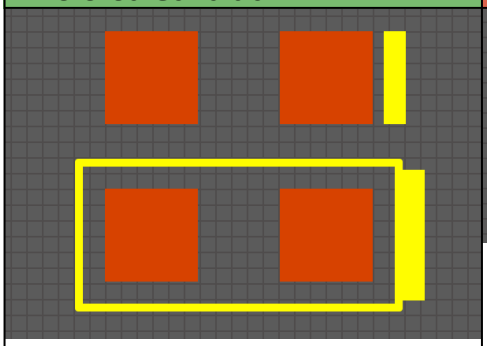
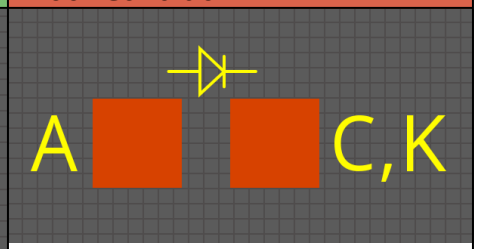
Silkscreen and Component IDs

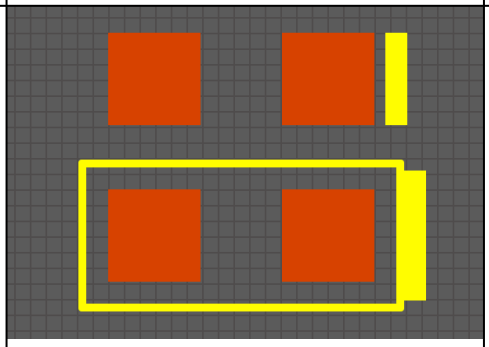
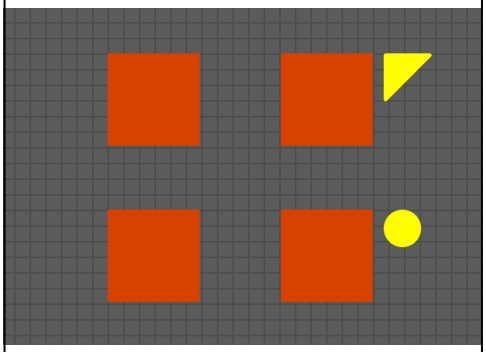
All component outlines on your silkscreen should be marked with a reference designator and polarity indicators (if applicable). It is important to make sure these designators and indicators are readable and visible even after components are installed for easy post-production verification. Figure 8 includes recommended guidelines on where reference designator locations and polarity markings should be placed on your silkscreen:

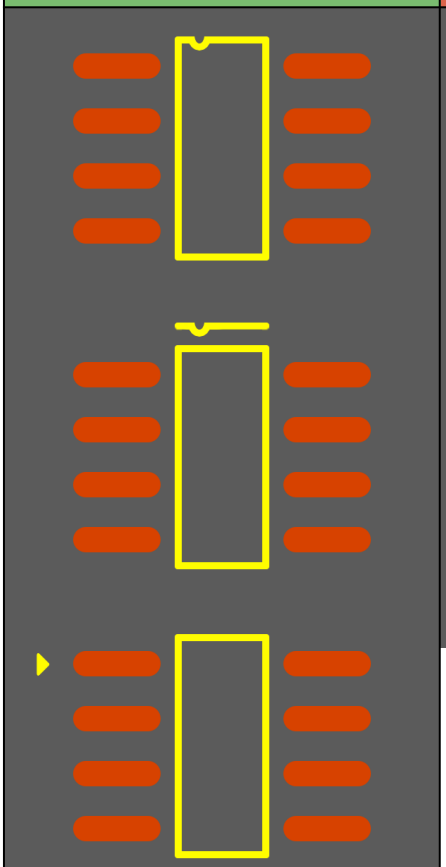
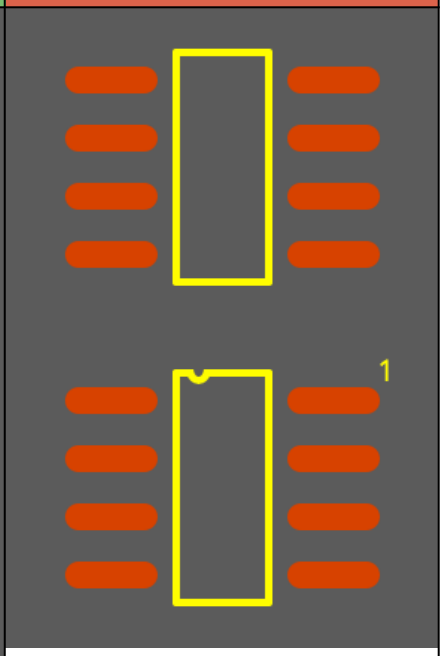
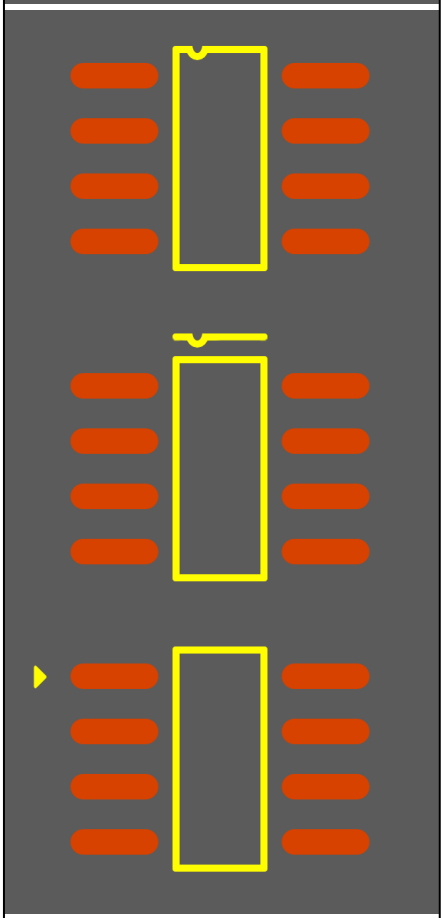
Component	Prefered Condition	Poor Condition
Chip Components		
	Always keep Silkscreen off pads as this might confuse the stencil printer vision system. Always take advantage of the Silkscreen high alignment tolerance to keep it off pads.	(Missing designators) Can't determine chip location, and would require documentation to determine designators. This could lead to increased cost due to increased inspection and potential component mis-loading.
		
	Chip location and pad pairs are denoted by Silkscreen line. Designators clearly identify location. Font should be increased when possible (especially for 0201 & 0402 devices)	
		
	Device orientation is same as text.	

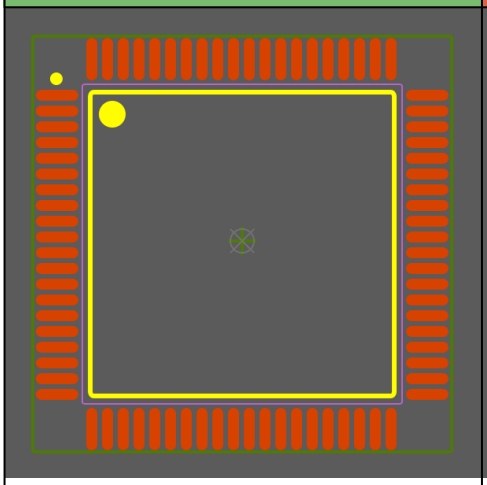
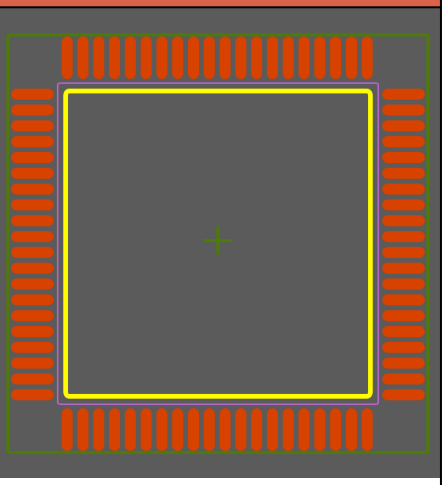
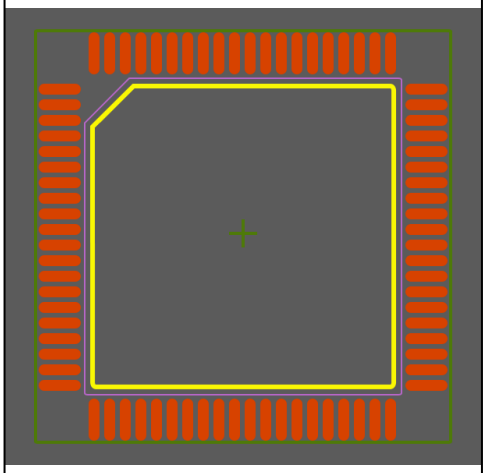
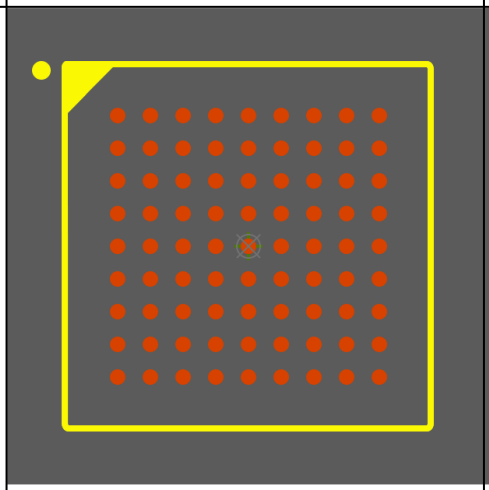
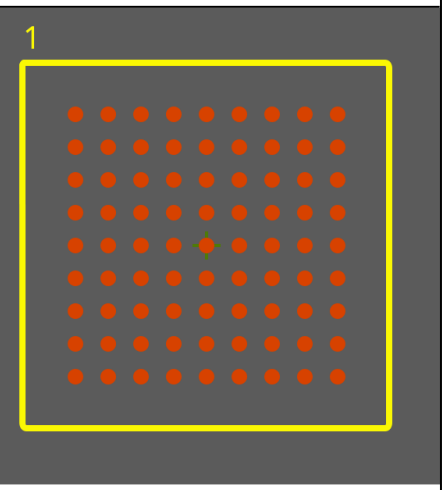
	Prefered Condition	Poor Condition
		
		
Text is same as device orientation. Via features should be avoided when placing reference designators on Silkscreen, as it become difficult/impossible to read for small devices (e.g. 0603, 0402, 0201)		
		

Polarized Capacitors	Prefered Condition	Poor Condition
		
	Mark the Anode (+) side of the capacitor on the silkscreen and it's best to use a bar that is equal to the pad's width. This will correspond to the line on the component (in general). A "+" or "dot" are fine for indicating polarity, however they don't represent the general standards for SMT polarized capacitors (which uses a line or a bar). From a manufacturer perspective, all that is important to them is to be able to align the component correctly rather than determining the Anode (or Cathode) orientation.	Unmarked polarized locations can complicate the assembly process, which can lead to delays to process the first article. Not to mention the danger associated with mounting a polarized capacitor in reversed orientation.

<table>
<tr><td>Diode</td><td>Prefered Condition
 
The Cathode end of the diode should be identified.</td><td>Poor Condition
 

Letters and diode symbol are poor methods of indicating polarity for manufacturers as they don’t assist with the manufacturing process.</td></tr>
<tr><td>LED’s</td><td> 
This is the standard method for indicating the Cathode on the silkscreen.
 
Although this chip style SMT indicates the LED’s polarity, it’s not the best as it becomes difficult to identify the orientation features for small chip LEDs (0603, 0402)</td><td></td></tr>
</table>

	Prefered Condition	Poor Condition
SOIC, SOP, SSOP, etc.		
		After the part is placed, the mark should be clearly visible.
	The away notch from the device allow for simple visual inspection after placement.	

<table>
<tr><td rowspan="3">QFP, TQFP</td><td>Prefered Condition</td><td>Poor Condition</td></tr>
<tr><td>  </td><td> 
</td></tr>
<tr><td>Large and easily found polarity mark.</td><td>Difficult to identify the polarity mark.</td></tr>
<tr><td></td><td>  </td><td></td></tr>
<tr><td></td><td>When component is placed, cut corner should be visible.</td><td></td></tr>
<tr><td>BGA</td><td>  </td><td> 
</td></tr>
<tr><td></td><td>BGA silkscreen outline should be a bit larger than the device.</td><td></td></tr>
</table>

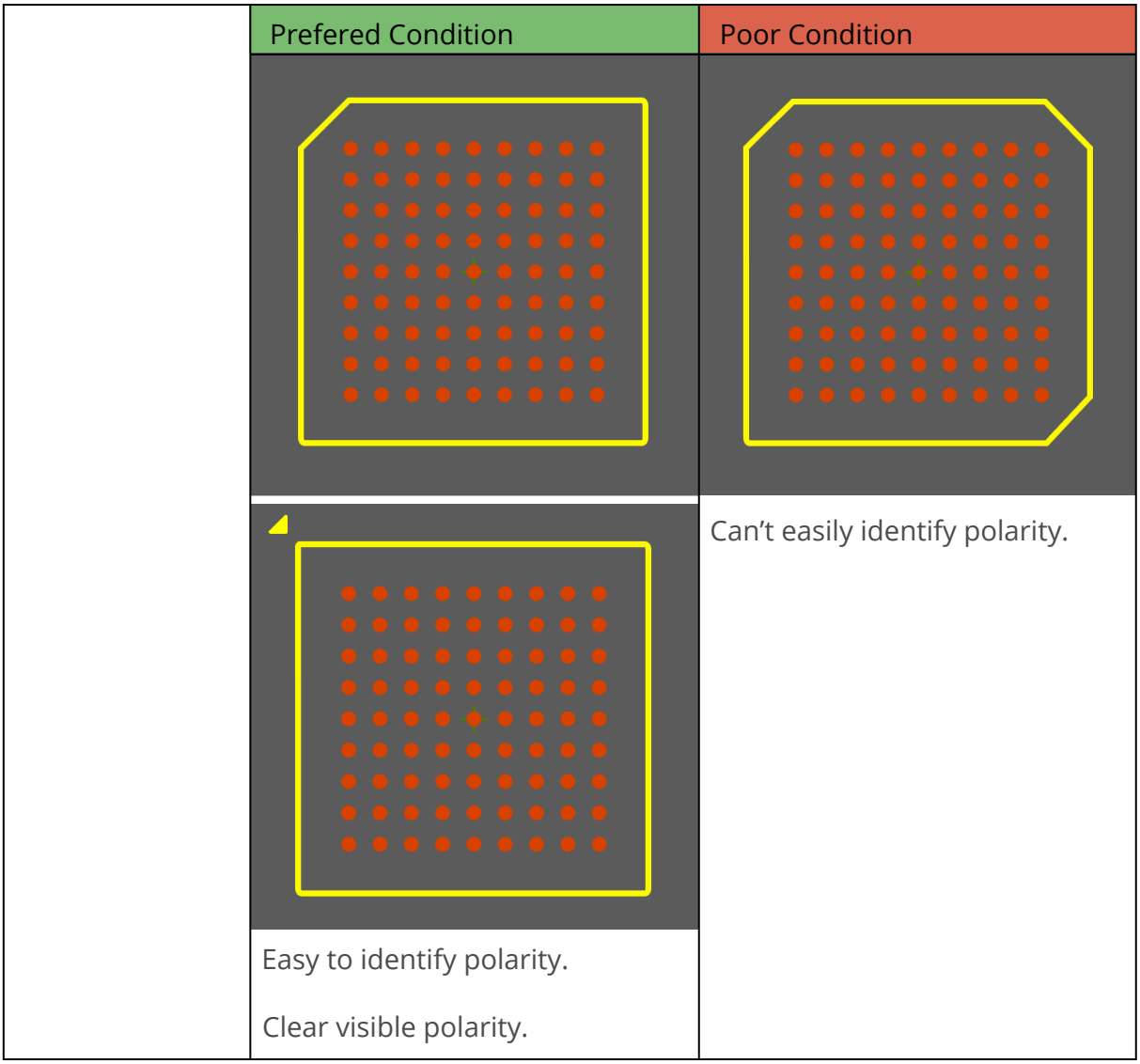


Figure 8 - Placement for Component Reference Designations

Component Reference Designators

Figure 9 includes a list of industry-standard reference designators from the IPC-2612[3-1] standart for schematic symbol generation. It is recommended to use these designators in all of your board layouts to help keep all of your projects consistent.

A	separably assembly	**LS**	loudspeaker, buzzer
AR	amplifier	**M**	meter
AT	attenuator, isolator	**MG**	motor-generator
B	blower, motor	**MH***	mounting hole
BT	battery	**MK**	microphone
C	capacitor	**MP**	mechanicalpart
CB	circuit breaker	**P**	connector, plug, male
CP	connector adapter, coupling	**PS**	power supply
CN	capacitor network	**Q**	transistor
D or CR	diode	**R**	resistor
D or VR	breakdown diode	**RN**	resistor network
DC	directional coupler	**RT**	thermistor
DL	delay line	**S**	switch
DS	display, lamp	**T**	transformer
E	terminal	**TB**	terminal board, terminal strip
F	fuse	**TC**	thermocouple
FD	fiducial	**TP***	test point, in-circuit test points
FL	filter	**TZ**	transzorb
G	generator, oscillator	**U**	inseparable assembly, IC pkg
GN	genera network	**V**	electron tube
H	hardware	**VR**	voltage regulator
HY	circulator, directional coupler	**W**	wire, cable, cable assembly
J	connector, jack, female	**X**	fuse holder, lamp holder, socket
K	contactor, relay	**Y**	crystal, magnetostriction oscillator
L	coil, inductor, bead, ferrite bead	**Z**	miscellaneous

Figure 9 - Component Reference Designators[3-1]

*Not a class letter, but commonly used to designate test points for maintenance purposes.

*Note: The above list is not exhaustive. See the standard list of class designation letters in **ANSI Y32.2/IEEE Std 315** [3-2], Section 22 and the Index.*

Solder Mask

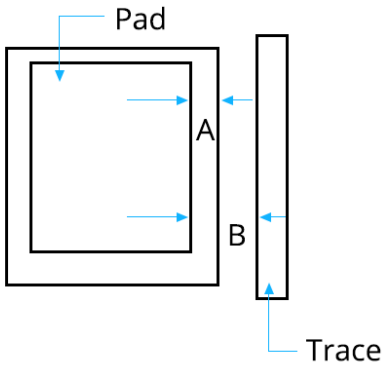
The solder mask is a thin, lacquer-like layer applied as a final coating to your PCB to protect various features including copper traces and ground planes that should not be soldered. Some of the benefits of solder masking includes:

- Protecting your PCB against oxidation damage.
- Preventing thieving and solder bridging (shorts) between conductors and lands.
- Preventing flaking during the assembly process if placed directly over bare copper.

Basic Clearance Requirements for Solder Mask

Wherever soldering or electrical contact is needed (around SMD and PTH pads, tooling holes, shield contact areas, fiducials, etc...) a solder mask clearance is required. Specifying a solder mask clearance ensures that there is no encroachment of the solder mask on pads during fabrication, which can result in a smaller solder fillet or completely disconnected pads if proper clearance requirements are not specified. Refer to Figure 10 below for proper clearance requirements for solder mask on pads and traces:

	A	B



	Minimum S/M Clearance per Side (mils)	Minimum spacing Pad to trace (mils)
Nomenclature	10	---
Screened requirements	7	---
Enthone DSR 3241	2*	5*

* IPC A600 Rev E class II and III acceptance requirement

In the example above, if minimum spacing between the pad and trace (column B) is less than required, then solder mask will be applied to the pad or exposed metal on the trace and could result in a board malfunction.

Solder Mask between SMD Pads

If there is a need for solder mask between SMD pads and there is not enough spacing to apply it, then it is recommended to keep two things in mind:

- The minimum spacing provided between the pads.
- The minimum successfully reproducible solder mask size your manufacture can make.

With these two requirements in mind, it is recommended to either increase the spacing between the pads for solder mask application or consult with your manufacturer to determine additional alternatives.

Vias and Holes

Vias are a critical part of every PCB design and are responsible for transmitting electrical current between layers. They can also be a significant burden to manufacturing costs if consistent clearance and sizing guidelines are not followed. The sections below will cover the specifics of via and hole clearances, sizing guidelines, and specific via applications.

Via Clearance Requirements

Standard vias should maintain minimum clearances from adjacent conductors, and the clearance will largely depend on whether the via is tented or exposed.You will often find that exposed vias will require greater clearances to close exposed electrical connections when compared with masked vias.

Via Size Guidelines

When designing plated via holes, it is recommended to maintain a 1:1 aspect ratio between the hole diameter and the substrate thickness. This rule of thumb will ensure that adequate copper metal builds up throughout the entire hole during the fabrication process. For example, in a 0.20” thick substrate, holes should at least 0.20” in diameter. However, most manufacturers have a wide selection of drill hole sizes and will usually meet requirement outside this general recommendation. One thing to remember when choosing a hole size is that a finished plated-through hole will be narrower due to the plating. Figure 11 depicts typical standard drill sizes:

Drill Number	Holes size	Finished Hole Size
70	.028”	.025”
65	.035”	.032”
58	.042”	.039”
55	.052”	.049”
53	.0595”	.056”
44	.086”	.083”
1/8”	.125”	.122”
24	.152”	.149”

Figure 11 - Standard Drill Sizes for Vias and Holes

Annular Rings

The annular ring is the difference between the pad diameter and the corresponding drill diameter; in other words, the area on the pad that surrounds the via. Figure 12 shows how to easily calculate the width of an annular ring:

Annular Ring Width = (diameter of the pad - diameter of the hole) /2

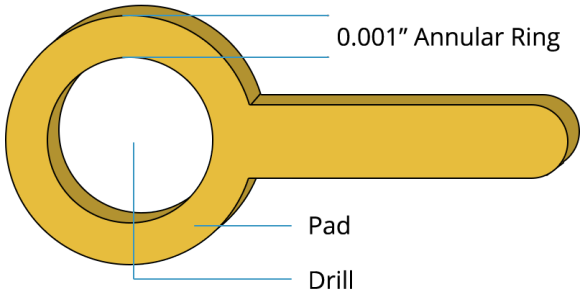


Figure 12 - Recommended Annular Ring Width

There are many conditions that can cause the drilled hole not to be exactly at the center during manufacturing. If it is acceptable to include “tangency” on the pads of your finished product, then it is recommended to check with your manufacturer on their guidelines for minimum annual ring widths.

To ensure a 0.001” minimum annular ring on the finished product, all pads on your design should be 0.0008” (2 x 0.0004”) larger than the drilled hole. This will ensure the drilled hole will be tangent to the pad’s edge. If you do not plate your design’s through-holes, it can result in smaller annular rings, which could result in the ring being lifted during soldering or breaking off during normal board operations. This occurs due to the lack of support from a plated barrel.

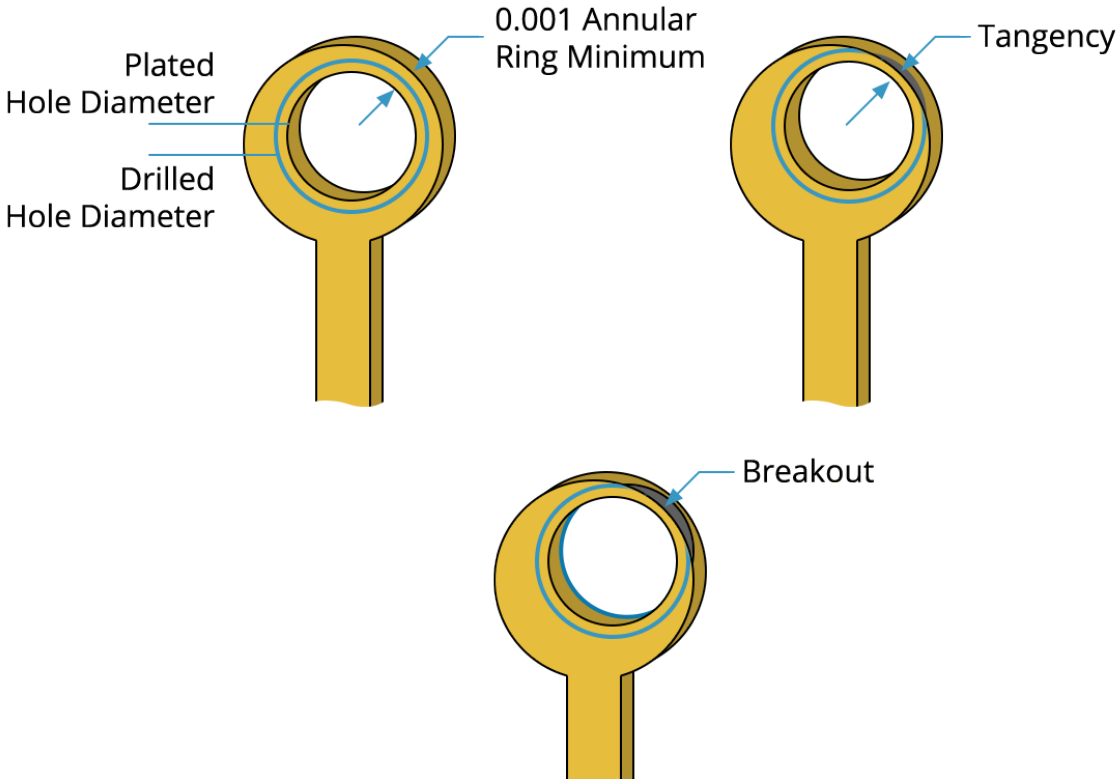


Figure 13 - Drilled and Plated Hole Diameters

Exposed Vias

Exposed vias are exposed electrical connections that are not covered with solder mask. Open clearances for exposed vias to other vias or lands not adjacent to the pad should be 0.15” at a minimum, with 0.20” being preferred.

Tented Vias

Tenting a via covers the via hole and annular ring with soldermask, and should be set as the default method in your design workflow. Keep in mind, there are usually no additional steps taken by your manufacturer to ensure a via opening remains closed. If you want to ensure that your via is closed and covered, you should specify in your fabrication print that you want these vias to be mask plugged, which is also called mask filled. This is especially important for BGA designs where vias are found close to the BGA’s SMD pads.
See Figure 14 for examples of recommended via tenting applications:

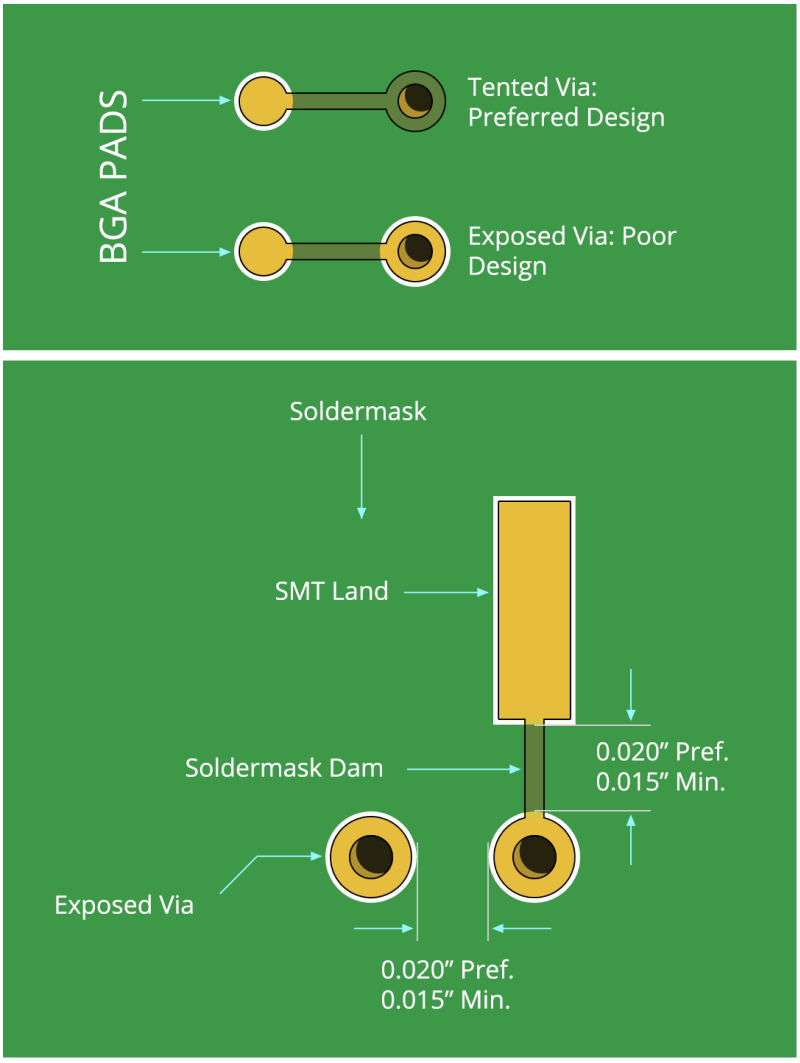


Figure 14 - Recommended Via Tenting Applications on a BGA

Via-in-pads and Micro Vias

Via-in-pads allows for close placement of bypass capacitors and makes routing easier for any ball pitch BGAs, as well as assists with thermal management and grounding. Follow the guidelines below when your design requires via-in-pads:

- The via-in-pads should be copper capped. In addition, the opposite side of the vias should be either copper capped (if used as an in-circuit test (ICT) point), or masked to ensure plating chemicals do not get trapped within the via.
- If the via-in-pads are not capped, additional assembly cost could incur to deal with solder wicking (redistribution of solder away from the intended joint) and solder scavenging (lack of enough solder and voids in intended joints).

Blind and Buried Vias

Similar to through-holes, blind and/or buried vias (BBV) are holes that connect one or more layers. In this process, a blind via connects an outer layer to one or more inner layers but not to both outer layers, and a buried via connects one or more inner layers, but not to an outer layer. This is important as these type of vias allow for denser boards and can save board real estate by not requiring any space on the components layers. See Figure 15 for an example of a blind and buried via application:

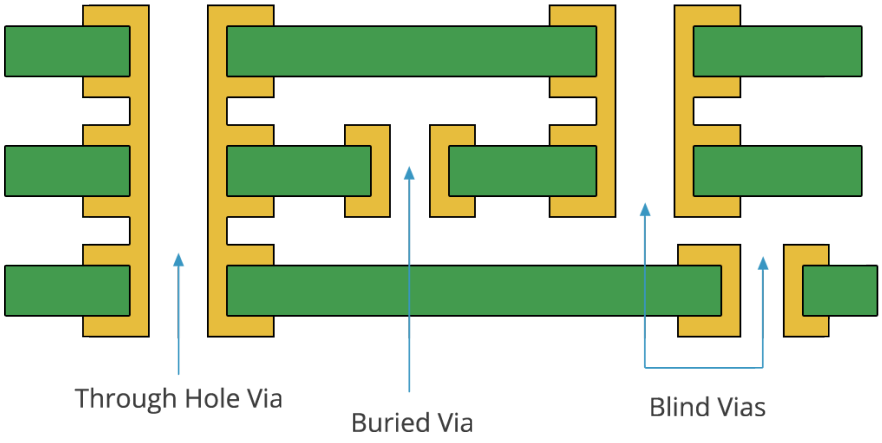


Figure 15 - Blind and Buried Vias

One particular detail to pay attention to when using blind vias is the drill depth (from an outside layer to an internal layer). For example, if you have a 0.062” thick board with 8 layers, the maximum depth of the blind via hole cannot exceed 0.018” (for a 0.035” via with a 0.018” hole).

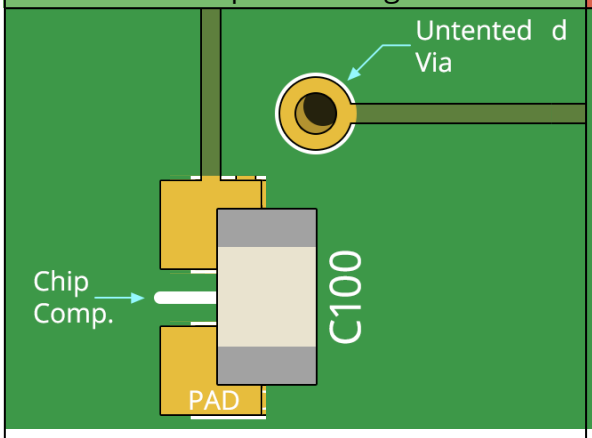
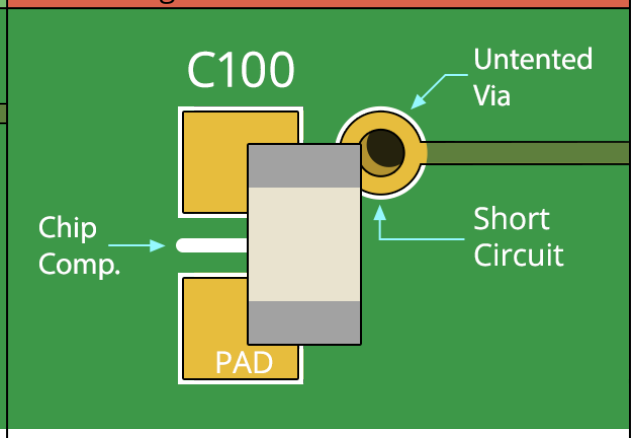
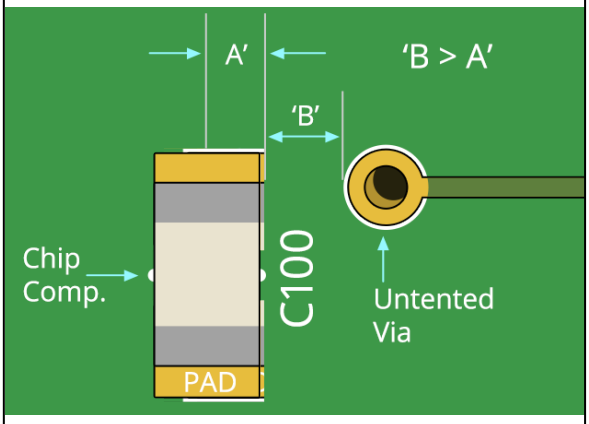
As a general guideline, keep internal layer’s via pads about 0.016” over the drill size, as this will provide a good yield for your manufacturer. It is recommended to consult with your manufacturer to further understand their BBV design constraints for copper weight, minimum drill size, and maximum aspect ratio requirements.

Vias Under BGAs

Reflow processes can cause chip components to shift or skew, resulting in one side of the chip component shorting to a nearby exposed via. Because of this, it is recommended that BGA vias be tented as a default in your design rules. Use the guidelines below for recommended clearance spacing for the exposed keep out area:

- If a via is adjacent to an SMD pad, it should be a minimum of 50% component termination width.
- If a via is at the end of an SMD pad, it should be at a minimum of 0.15” (preferably 0.20”).

Figure 16 show some examples of good design practices for vias that are placed near chip components:

<table>
<tr><th>Preferred/Acceptable Design</th><th>Poor Design</th></tr>
<tr><td> 
</td><td> 
</td></tr>
<tr><td>Ideal: maintain a 0.020 clearance (from via annular ring to adjacent conductor)</td><td>Poor: Shifted Chip component which can cause a short to an unintended via.</td></tr>
<tr><td> 
</td><td></td></tr>
<tr><td>Acceptable: ‘A’ is greater than ‘B’.</td><td></td></tr>
</table>

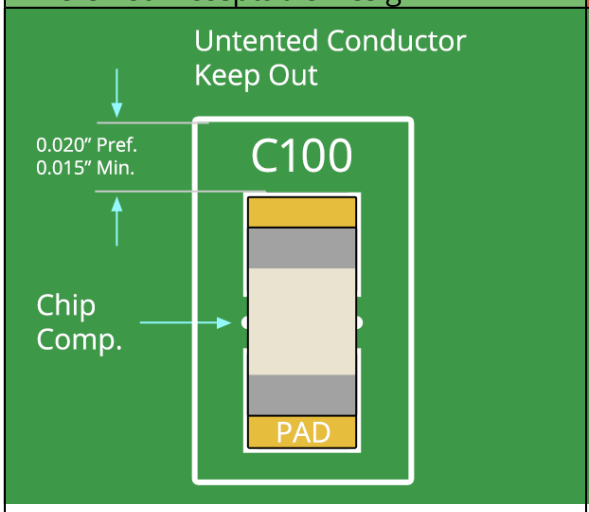
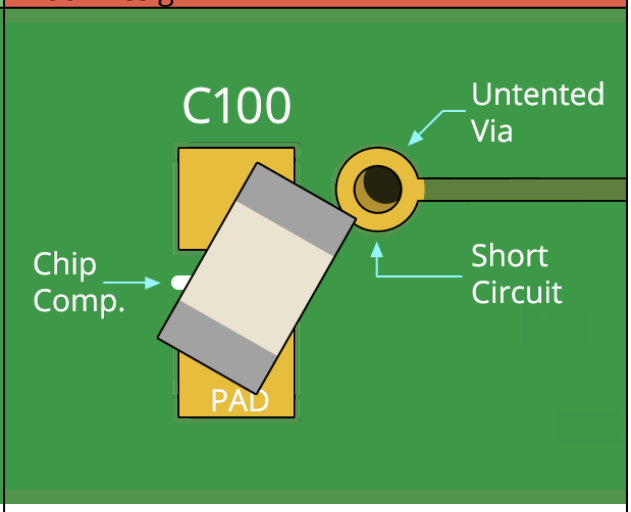
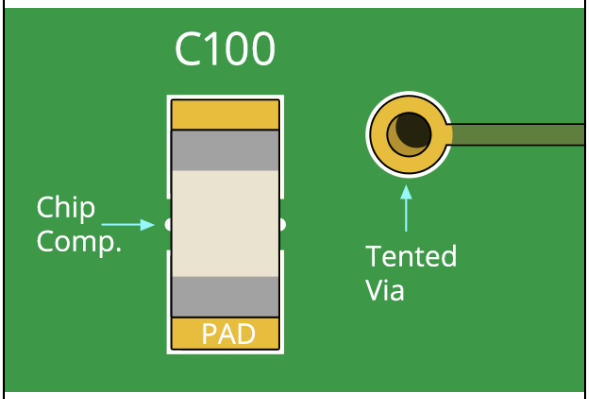
Preferred/Acceptable Design	Poor Design
	
Ideal: maintain a 0.020 clearance (from via annular ring to adjacent conductor).	Poor: Skewed chip component which can cause a short to an untended via.
	
Acceptable: Although via is within chip component keep-out area, it's tented.	

Figure 16 - Via Placement Guidelines Near Chip Components

Teardrop Pads

The purpose of adding a teardrop pad is to reduce the mechanical and thermal stress where the trace joins the pad by providing additional copper/metal support. This also helps to ensure that good connections are made and maintained as it increases the PCB manufacturer's tolerance when an order is drilled and a misregistration occurs.

The tear dropping process involves adding copper to the junction of an existing pad and a trace exit. It is important to primarily add these to through-hole drills, where you might have a small trace-to-pad ratio. They should also be added to circuit runs from a pad (solid or via pad), and this practice becomes more important as a trace narrows. For traces larger than 0.20", teardrops are usually not needed. As a rule, if your design is not an RF or high-frequency device, add tear drops at the final stage of your design. Figure 17 shows various teardrop examples and their recommended spacing and shape requirements:

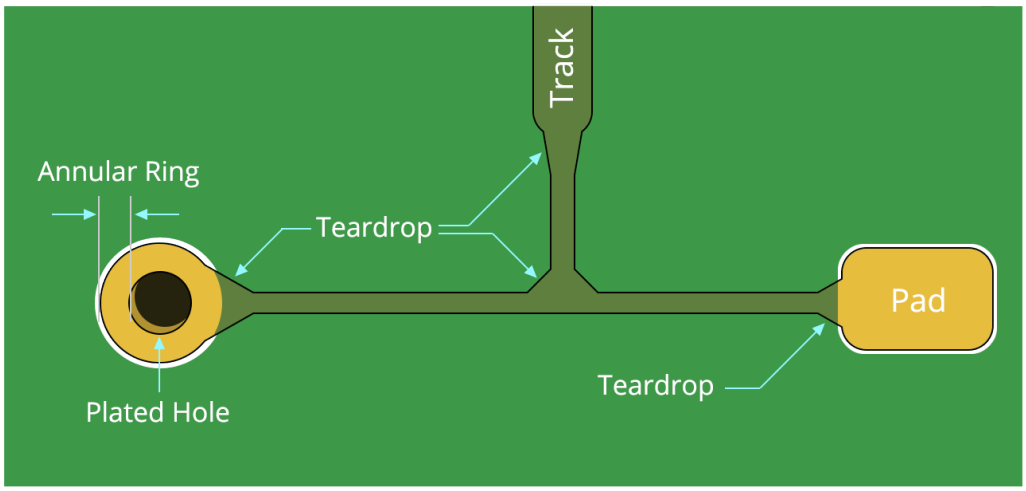


Figure 17 - Recommended Teardrop Shapes

Aspect Ratio Plating

Aspect ratio is the ratio between the thickness of the board and the size of the drilled hole (before plating)[3-4]. TThis ratio will guide your manufacturer so they do not exceed the mechanical capabilities of their drilling equipment. Figure 18 shows a visual example of how aspect ratios are determined on a PCB:

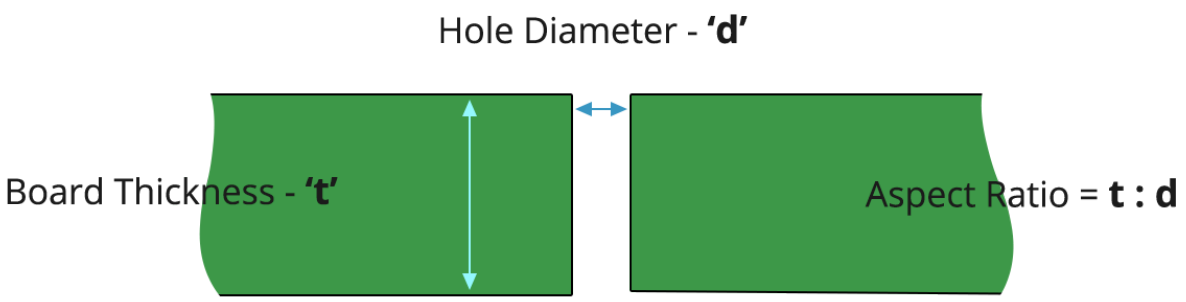


Figure 18 - Determining an Aspect Ratio for a PCB

For example, a PCB that has 0.065" thickness and consists of a hole size of 0.020" will have an aspect ratio equal to 3:1. This ratio is important as it relates to the plating process as well. Hole sizes that are too small compared to the board thickness (higher aspect ratios), might not achieve an acceptable copper plating when the plating solutions flow through the hole. Figure 19 provides a general set of guidelines for establishing aspect ratios:

Drilled	Board Thickness (mm)/Aspect Ratio			
Hole Size mm (inch)	1.8 (0.070”)	2.35 (0.093”)	3.15 (0.125”)	6.75 (0.125”)
1.65 (0.065”)	OK	OK	OK	4.1 : 1
1.65 (0.065”)	OK	OK	OK	5.9 : 1
1.65 (0.065”)	OK	OK	OK	7.6 : 1
1.65 (0.065”)	2.8 : 1	3.7 : 1	5.0 : 1	10.6 : 1
1.65 (0.065”)	3.5 : 1	4.65 : 1	6.25 : 1	13.3 : 1
1.65 (0.065”)	3.9 : 1	5.1 : 1	6.9 : 1	14.7 : 1
1.65 (0.065”)	4.4 : 1	5.8 : 1	7.8 : 1	
1.65 (0.065”)	5.2 : 1	6.8 : 1	9.3 : 1	
1.65 (0.065”)	5.6 : 1	5.6 : 1		
1.65 (0.065”)	7 : 1	9.3 : 1		

Figure 19 - Aspect Ratio Matrix for Specific Board Thicknesses[3-5]

Via Spacing, Placement, and Routing Guidelines

With your via sizing and types established, it is now time to start placing and routing them on your board layout. Below you will find several placement guidelines to keep in mind, especially for board layouts that utilize through-hole components or SIP-type packages.

Via Placement Recommendations for Through-hole Components

When your design consists of through-hole components, it is recommended to keep vias away from these devices as the via can cause the solder to flow up and damage those components. It is also recommended to keep vias away, around 0.100”, from SIP packages, as these packages can be incorrectly inserted.

General Via Placement Recommendations

Since solder can flow up through vias, it is not recommended to place vias under chip components as this can result in a damaged, shorted, or lifted component. This is also important because sometimes chip components need to be glued or epoxied to the board, and a via under it or near it can interfere with that area (see Figure 20 for an example).

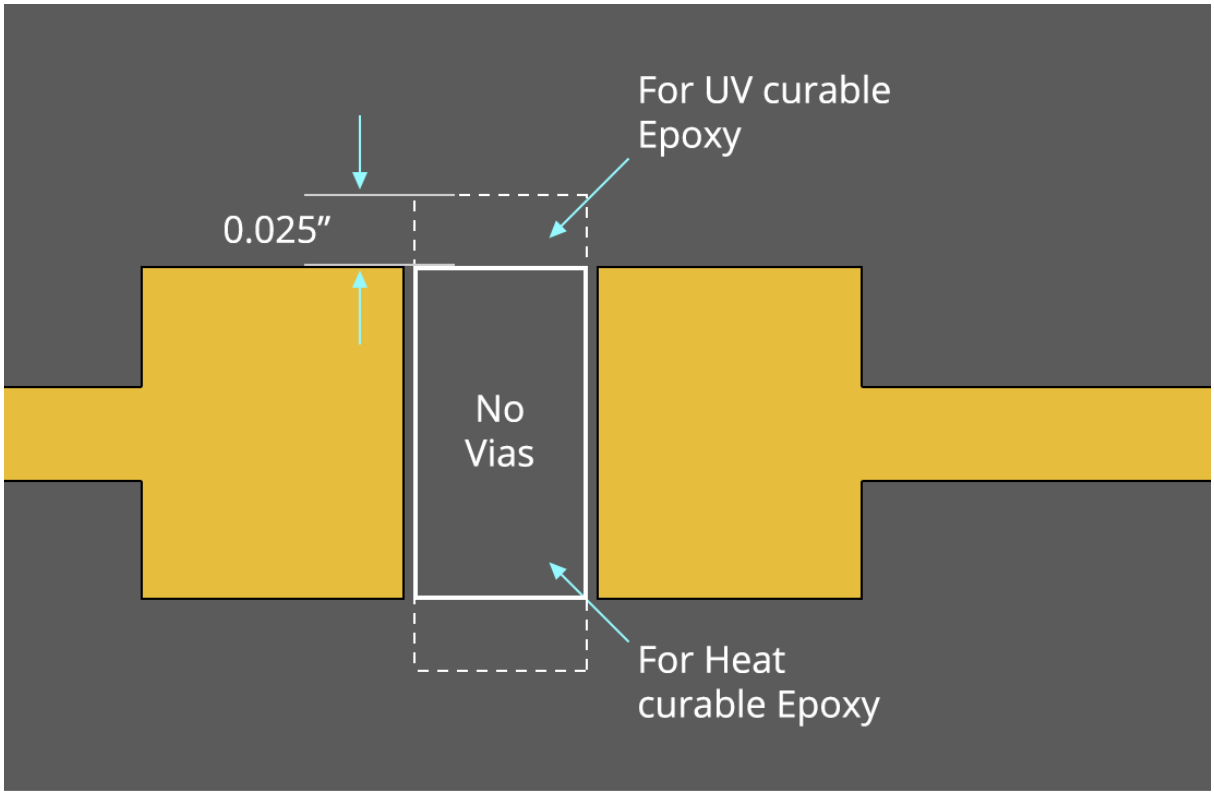


Figure 20 - Via Clearance Guidelines for Wave Soldering

When connecting a via edge to a component pad edge, clearances of less than 0.010” are not recommended unless you are designing a dense board. If your board is dense, then you will need to cover them with solder mask. It is recommended to consult with your manufacturer on the minimum clearances they require for denser boards. See Figure 21 for an example of recommended connections of vias to component pads:

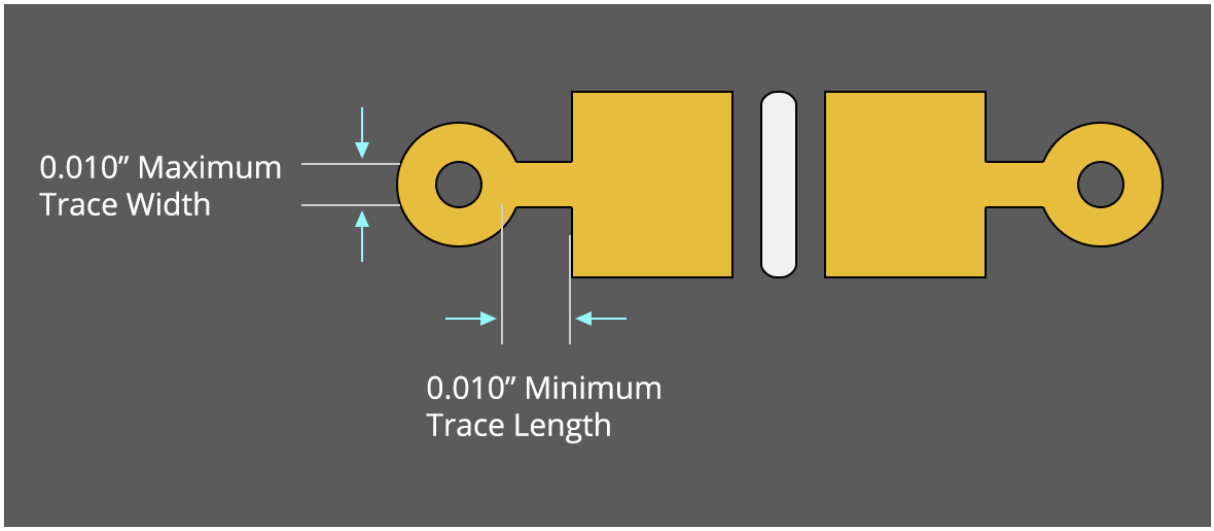


Figure 21a - Recommended Connections of Vias to Pad Components (Good Design)

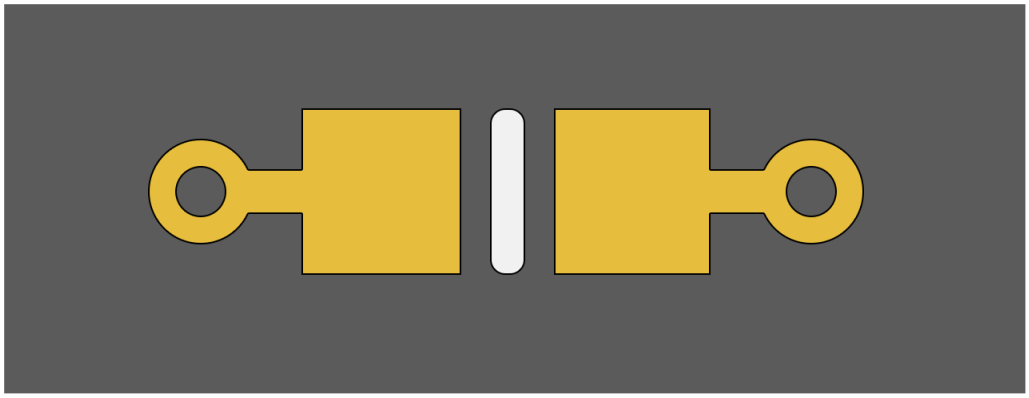


Figure 21b - Not Recommended Connections of Vias to Pad Components (Poor Design)

When not connecting a via to a component pad, a minimum of 0.025” clearance spacing is recommended, and this clearance should be increased to 0.040” if the via is on the solder side of the board.
See Figure 22 and make note of the wave solder direction:

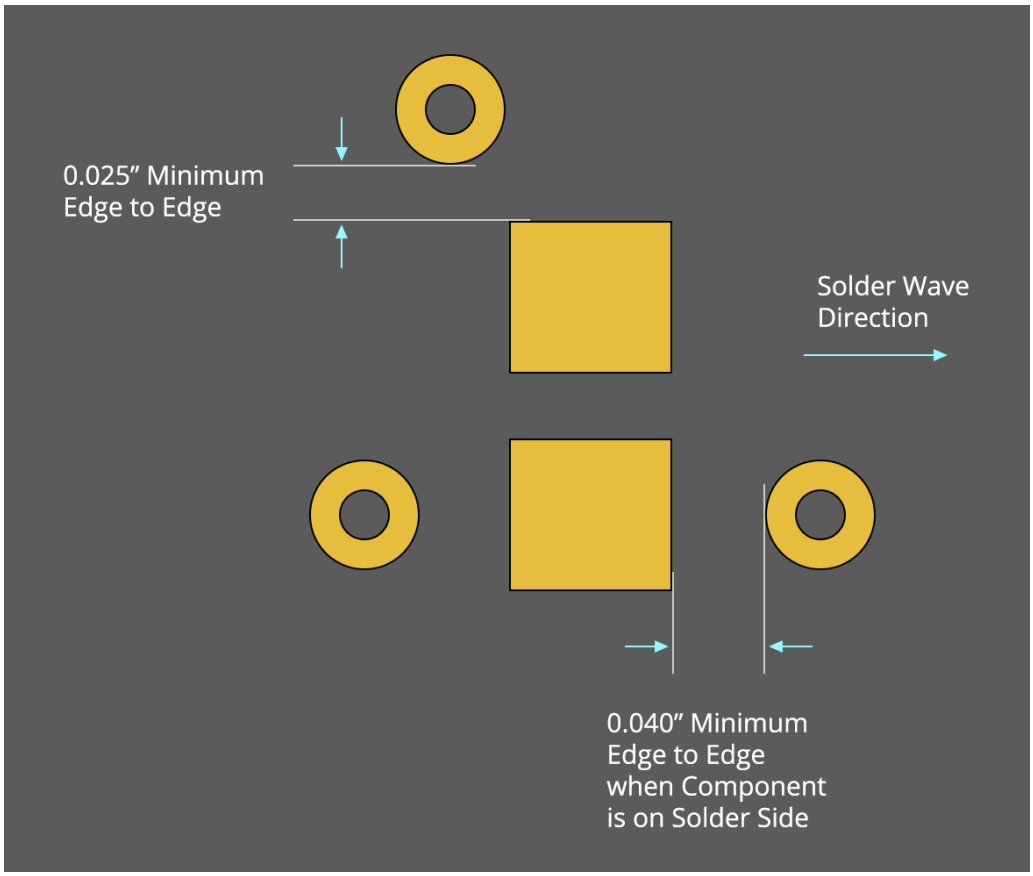


Figure 22 - Via Component Spacing for Wave Soldering

Finalizing Your Via Requirements

Vias are a critical piece of every electronics design and ensuring that your clearances, sizing, types, and routing methods remain consistent throughout your board will go a long way towards designing a manufacturable and cost-efficient board. The next section will focus on additional board layout strategies and other options to be aware of during your design process.

Trace Routing to Component Lands

When you have a component's termination that could generate heat and is connected to a large trace, the heat transfer produced can lead to a poor solder joint. This can even result in open solder joints for connections without a solder mask, as solder can migrate away from the component termination.

To resolve this issue, trace necking can help with thermal balance and prevent the solder and heat from flowing away from the pad.

Necking a Trace

A general guideline for necking a trace is to keep it no wider than 0.010" where it connects to the pad and run it at least 0.010" before it connects to the large trace. If you have to connect a wide trace to a component land, they should have the same width while keeping the dimensions as small as possible. Figure 23 shows an example of this process:

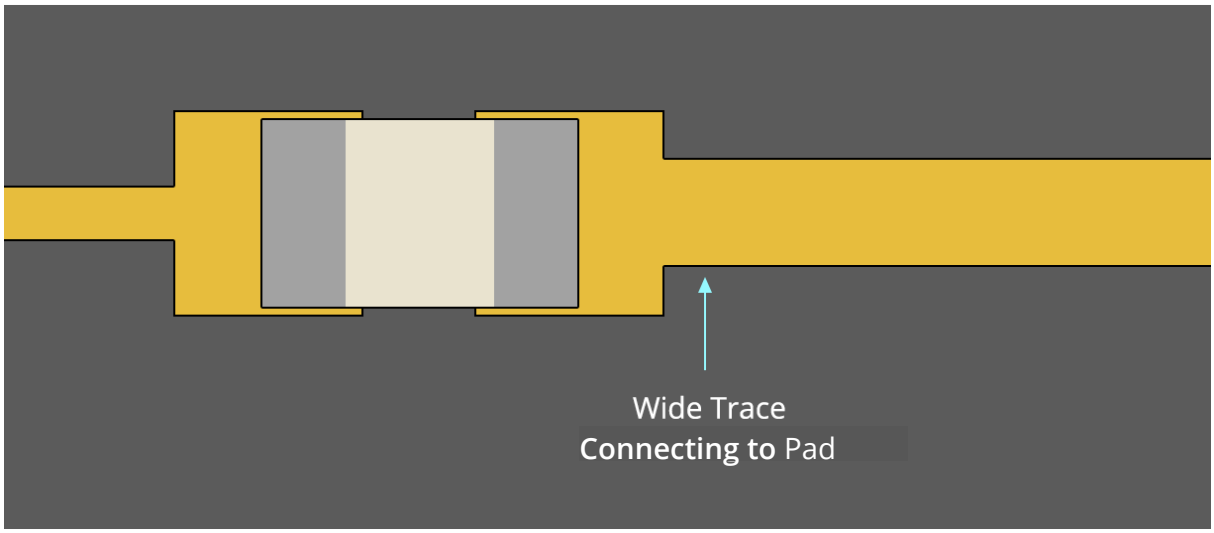


Figure 23b - Connecting Large Traces to Component Lands (Good Design)

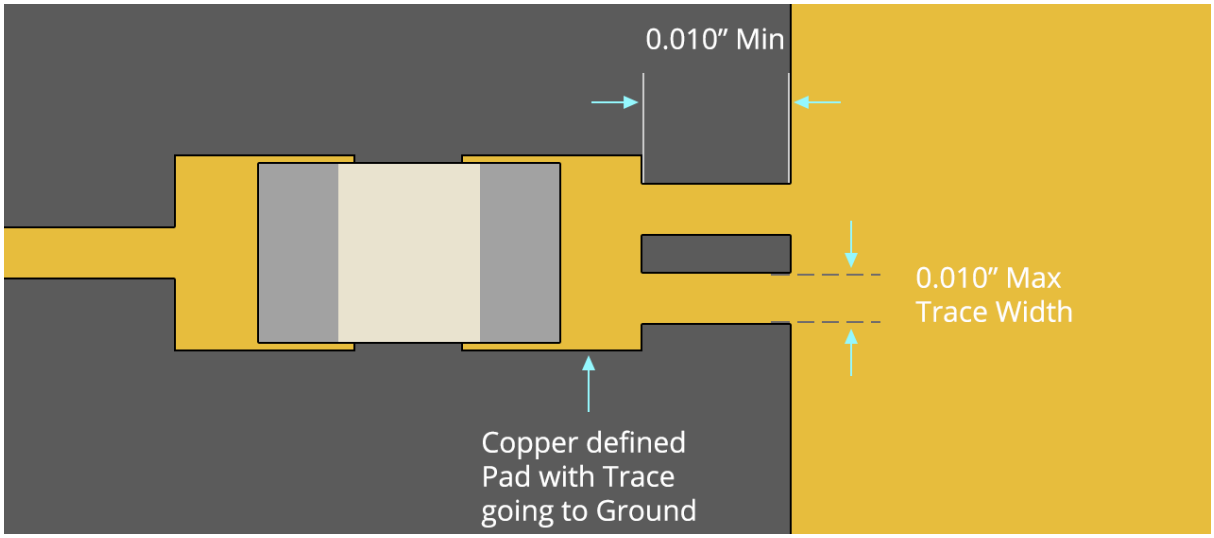


Figure 23b - Connecting Large Traces to Component Lands (Good Design)

Connecting Large Ground Traces to Component Lands

When you need to connect large ground traces to component lands, you should neck down the traces to ensure a good balance and to prevent heat transfer that might cause solder to travel to the large conductor area. You can also have multiple traces connecting land patterns to the large traces and ground planes. It is recommended to keep trace width (when necking) from the pad at a max of 0.010” and 0.010” as a minimum length from the pad to a large plane or trace. See Figure 24 for an example of these spacing recommendations:

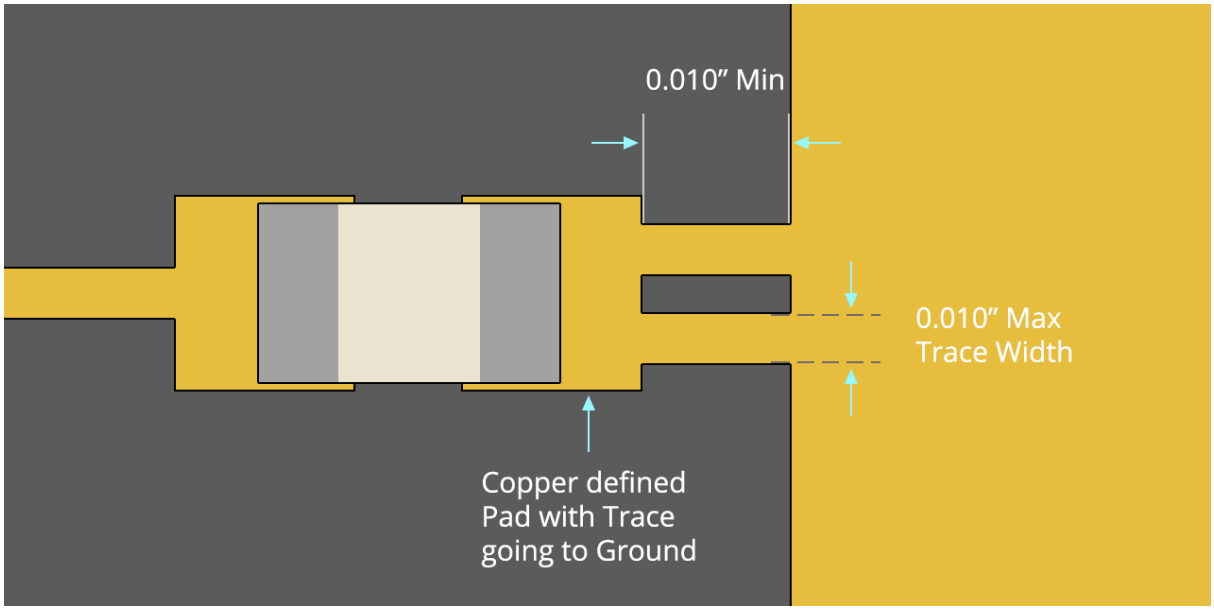


Figure 24a - Connecting Component Lands to Large Conductors (Good Design)

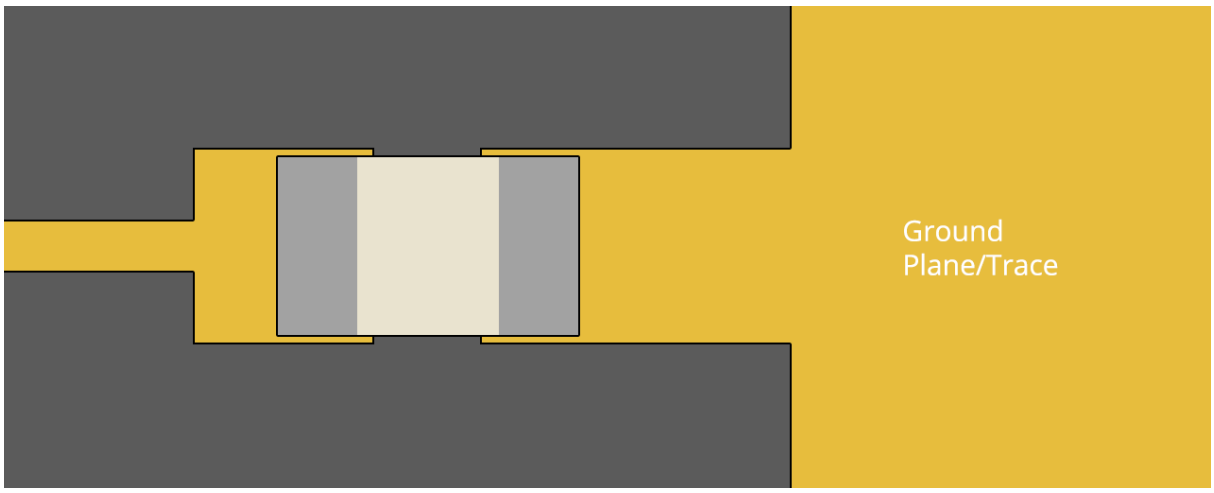


Figure 24b - Connecting Component Lands to Large Conductors (Poor Design)

Connecting Pads of Closely Spaced Components

When connecting the pads of closely spaced chip components, it is recommended to route the traces out across and then back into the pads rather than having traces routed directly between the pads or across the pads. This will help prevent shorts that will be mistakenly reworked, prevent tombstoning due to poor thermal balances, and avoid cold solder joints and shifting of components. See Figure 25 for an example on how to properly connect pads to components:

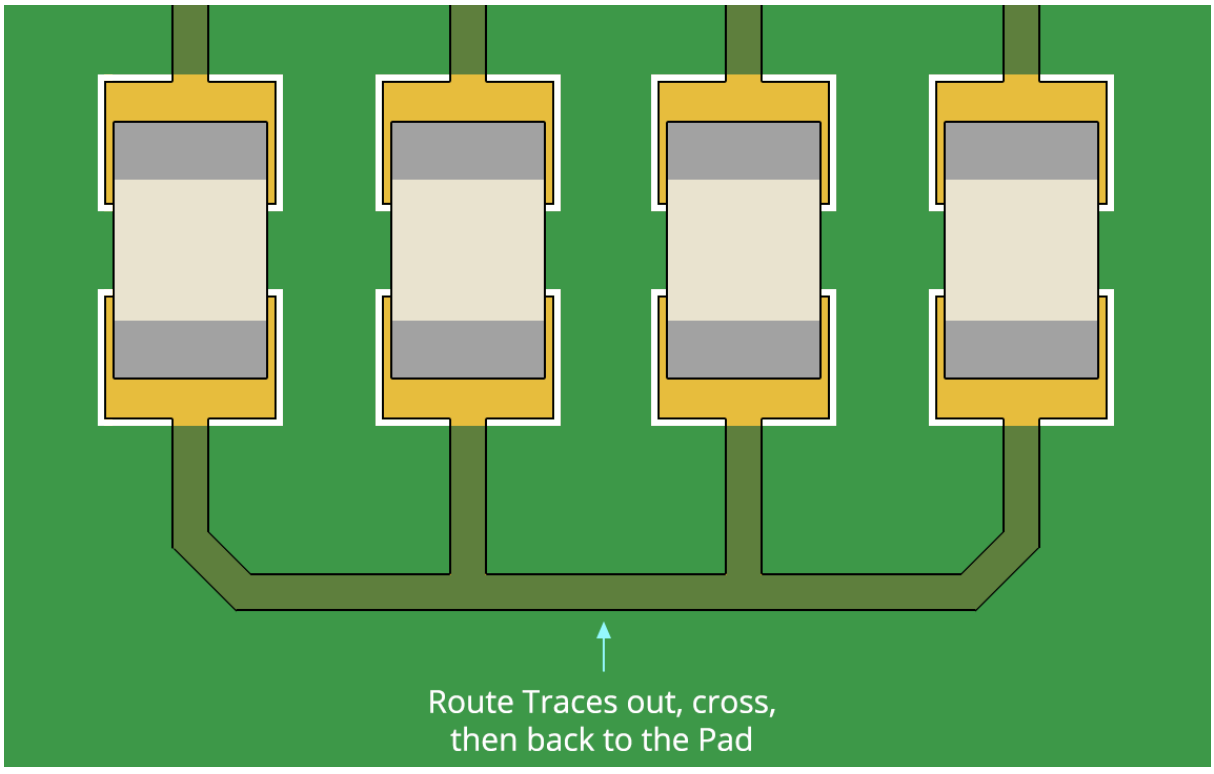


Figure 25a - Connecting Pads of Closely Spaced Components (Good Design)

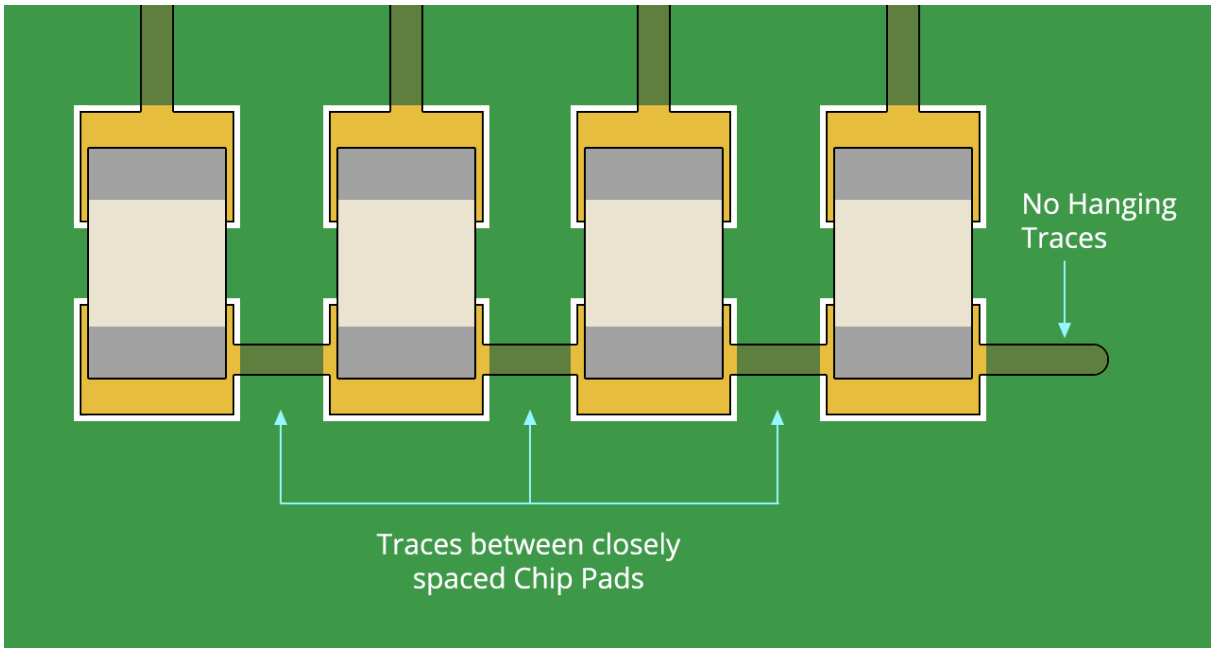


Figure 25b - Connecting Pads of Closely Spaced Components (Poor Design)

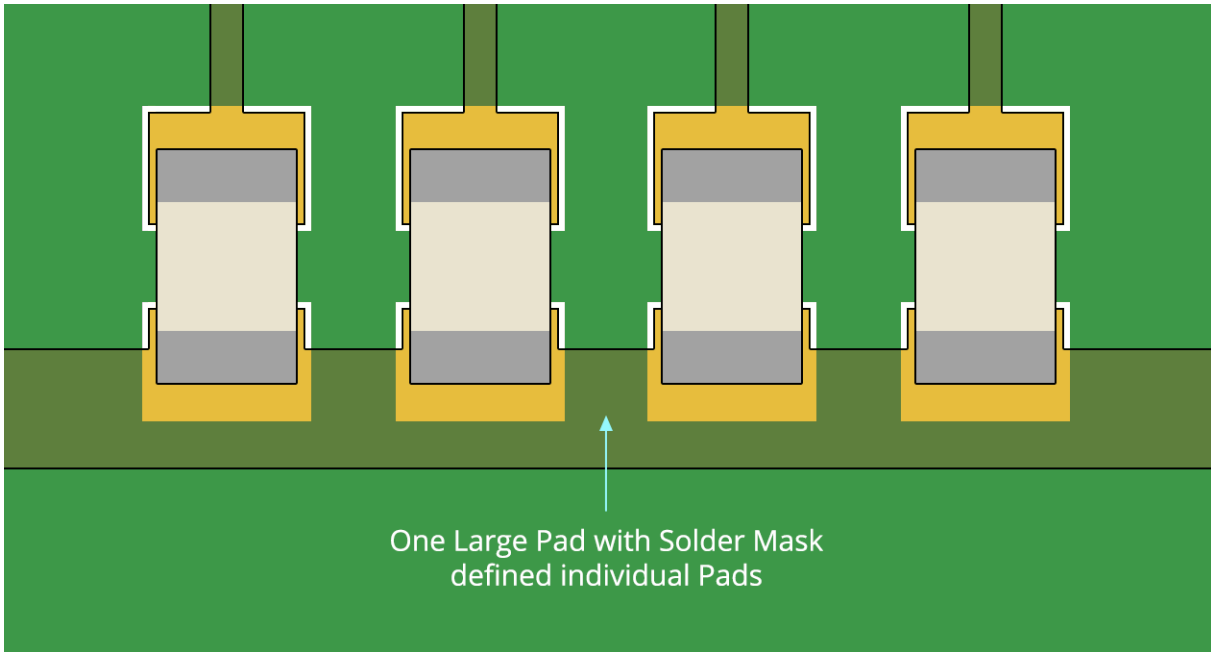
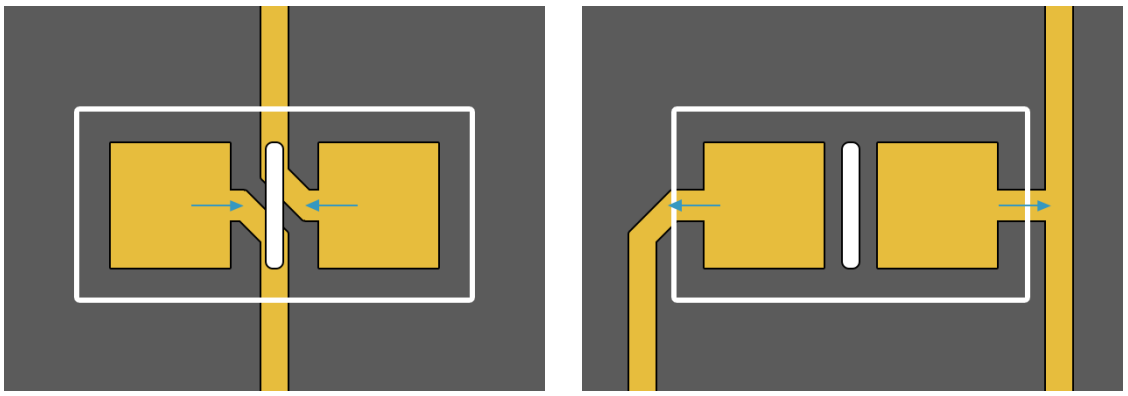


Figure 25c - Connecting Pads of Closely Spaced Components (Poor Design)

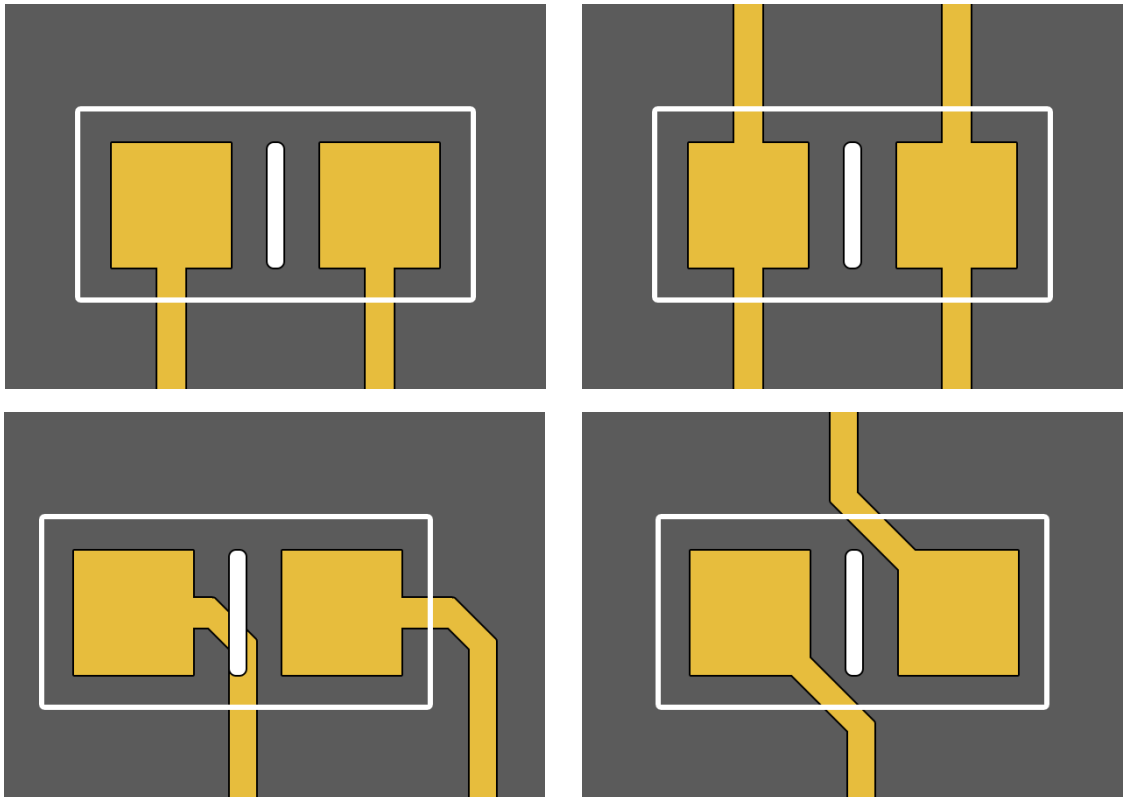
Connecting Pads to Traces

Every pad should be connected to its own trace, and it is recommended to have the routing from either outside the edges or inside the edges of the pads while keeping the routing symmetrical. This is important and critical in areas with no soldermask, as it helps prevent the solder from moving away from the pad and stops components from shifting. In general, most manufacturers will want to see a balanced amount of copper connecting the component pads. See Figure 26 for trace routing examples and preferred methods of connecting traces to chip pads.

Preferred Routing: (arrows indicate solder migration)



Acceptable Routing:



Non-Preferred Routing: (arrows indicate solder migration)

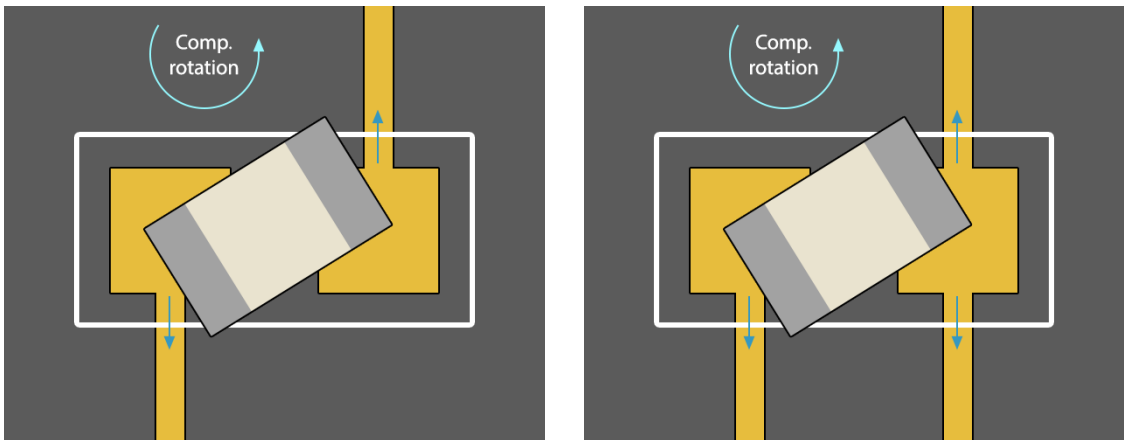


Figure 26 - Connecting Traces to Component Lands When Using Soldermask

When routing leaded SMD components, it is recommended to route the trace over and then back in, forming a flipped “U” configuration, rather than forming an “H” by going directly between lands. See Figure 27 for an example of this “U” shaped configuration:

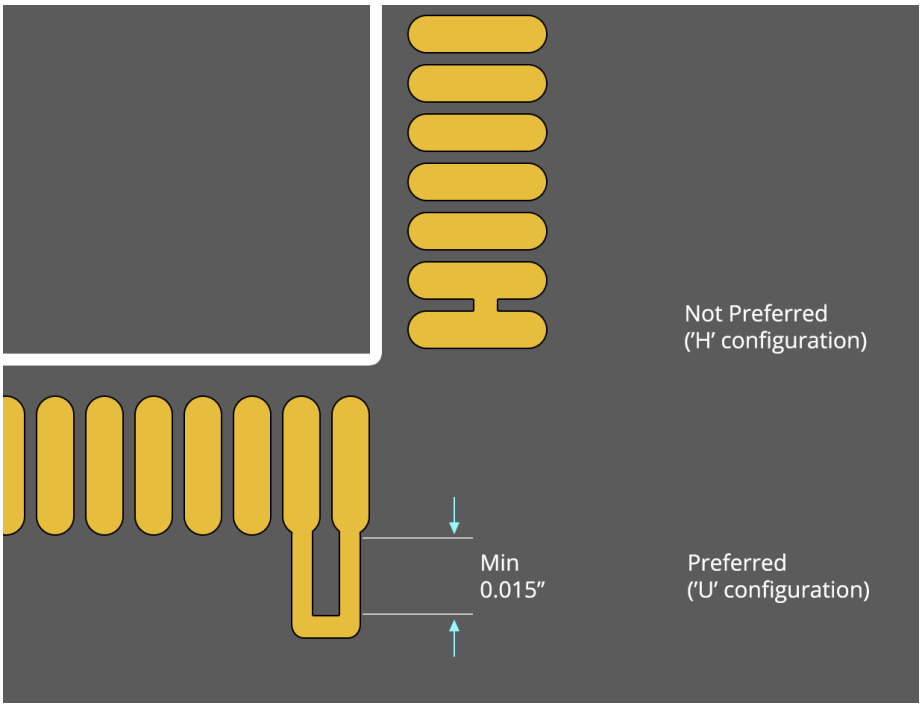


Figure 27 - “U” Configuration for Routing Leaded SMD Components

Planes and Traces

It is recommended to have your power and ground planes always on internal layers, symmetrical, and centered. This will help prevent your board from bending, and will also help with accurate positioning and component placement. Most assembly manufacturers allow a bow and twist of 0.7%-0.75% either for double layer PCBs or multilayer PCBs with 0.06” board thickness.

The same set of recommendations applies to traces. They should be as equally laid out as possible in both the X and Y axis and preferably in multi-orientation on all layers to help prevent board warping.

Plating Options

For plated through-hole (PTH) boards, electroless copper is utilized to make the hole path conductive enough to allow further build-up of copper metal to a thickness specified by the designer, which is usually 0.001”. The electroless copper process also adds an average of 0.0013” of copper to the external lines, in addition to the original copper foil (0.5 oz or 1 oz). Figure 28 summarizes the most common finish types for all exposed circuitry on a board. It is recommended to consult with your manufacturer for guidance on selecting a finish that will lessen material decay and improve surface consistency when connecting components on your board.

Final plating finish comparisons

	HASL (SnPb)	HASL Lead-Free	Electroles nickel immersion gold- ENIG	Immersion Silver- IAg	Organic Solderable Preservative - OSP	Immersion Tin - ISn	Electrolytic nickel gold - NIAu
RoHS Compliant	No	Yes	Yes	Yes	Yes	Yes	Yes
Fabrication costs	Low	Low	Medium	Medium	Low	Medium	High
Shelf life	1 Year	1 Year	1 Year	9-12 Months*	9-12 Months*	9-12 Months*	1 Year
Assembly cyde capacity	Multiplie	Multiplie	Multiplie	Multiplie	Multiplie	Multiplie	Multiplie
Multiplie rework capacity	Limited	Limited	Limited	Yes	No	No	No
Solder wettability	Excellent	Good	Good	Very Good	Good	Good	Good
Co-planarity	Poor	Good	Excellent	Excellent	Excellent	Excellent	Good/Poor
Solder joint integrity	Excellent	Good	Good	Excellent	Good	Good	Poor**
Low resistanse/ high speed	No	No	No	Yes	N/A	No	No
Aluminium wire bond	No	No	No	No	No	No	Yes

* Requires unique storage techniques

** Thicker applications of Au can cause embrittlement

Figure 28 - Final Plating Finish Comparisons[3-6]

Thermal Relief

Thermal relief is critical for wave soldering, SMT processing, and hand soldering. This becomes more important on high copper content assemblies and multilayer boards as the copper can turn into a heat sink that draws most of the heat from the soldering areas. This can make it difficult to maintain process temperatures, and the presence of a thermal relief makes it easy to solder through-hole components by slowing the rate of heat sinking through plated through-holes. Not having a heat relief could result in poor hole filling and cold solder joints, and can also impact rework capabilities. Some of the benefits of adding a thermal relief on your board include:

- Better control over hole size.
- More consistency in plating thickness.
- Faster and easier solder joint inspection.

As a general rule, it is recommended to use a thermal relief pattern for any via or hole that is connected to a ground or power plane. It is also recommended to avoid using thermal relief on press fit component holes and consider using the thermal current capacity in your calculations. See Figure 29 for an example of a typical thermal relief pattern on a board layout:

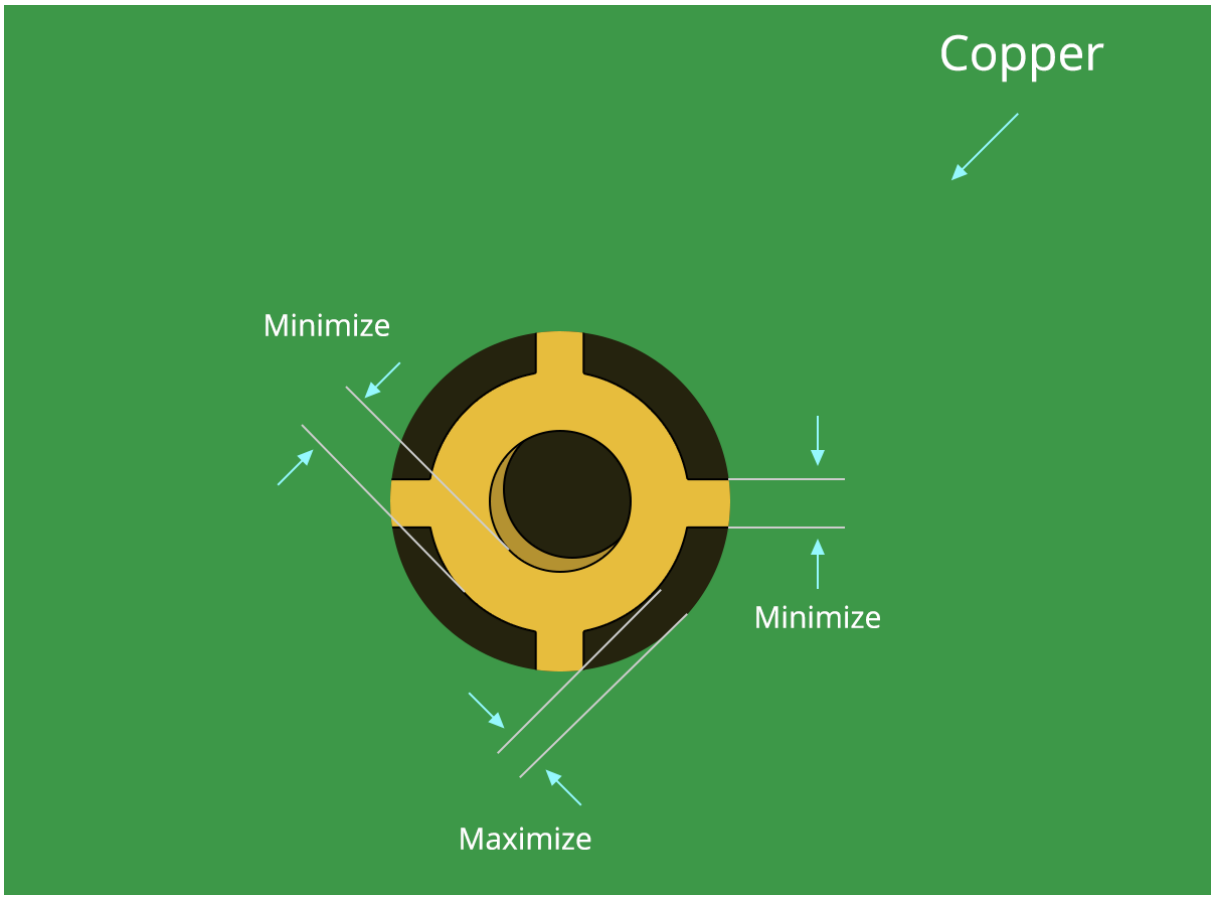


Figure 29 - Typical Thermal Relief Pattern

Laying the Groundwork

This chapter laid the groundwork for your design process, allowing you to strategize the basics of your board layout including using through-hole or SMT for components, clearly documenting your silkscreen, understanding the importance of solder mask, and finally specifying via sizing and placement. We are now ready to dive into the specific guidelines for component placement and orientation on your board layout to have your PCB successfully manufactured.

Placing and Orienting Your Components

Introduction

With your preferred component types established, it is now time to decide how to place efficiently and orient those parts on your board. This process will have a large effect on how you utilize the available space on your board layout, and can be one of those most challenging steps in your design process. Below you will find specific recommendations on how to optimize your component placement to be both manufacturable and capable of meeting your specific design requirements.

General Component Placement and Spacing Guidelines

Before going into the specifics of component placement and orientation, there are several general guidelines to keep in mind:

- For efficient soldering and placement, it is recommended to orient similar components in the same direction.
- Avoid placing components on the solder side of a board that would lay behind components with plated through-holes.
- To minimize the number of processes required to assemble a board, try to place all your SMD components on the same side of the board, and all the through-hole components (if mixed) on the top side of the board.
- When you have mixed technology components (through-hole at the top and SMT on both sides), manufacturers might require an extra process to epoxy the bottom components which will add to your overall manufacturing costs.
- You should terminate all lands with only one trace, and define your pads with solder mask.

By following the above guidelines alone, you will be well ahead of a typical PCB designer in the efficient utilization of your board layout while also ensuring that your board is manufactured without any delays. The next sections will go into specific component placement, orientation, and termination recommendations.

Specific Component Placement and Board Orientation Guidelines

Having adequate spacing between your components is critical for proper soldering, performing rework, testing your board, and a smooth assembly process. Poor spacing on components could lead to manual placement due to the inability of a pick-and-place machine to do its job properly.

Sometimes you cannot avoid scattering chip components on the bottom of your board. To avoid shadowing and unsoldered termination, it is recommended to have a 0.100” spacing between each component, as shown in Figure 30:

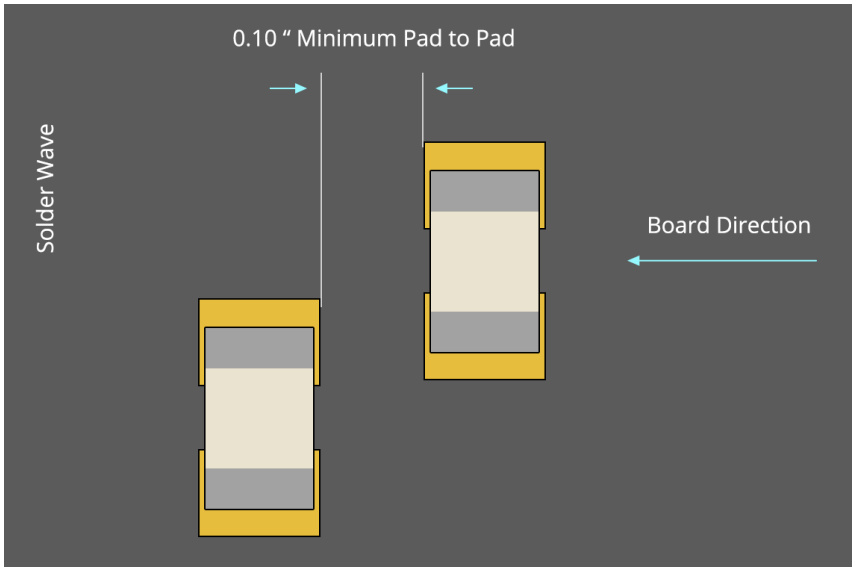
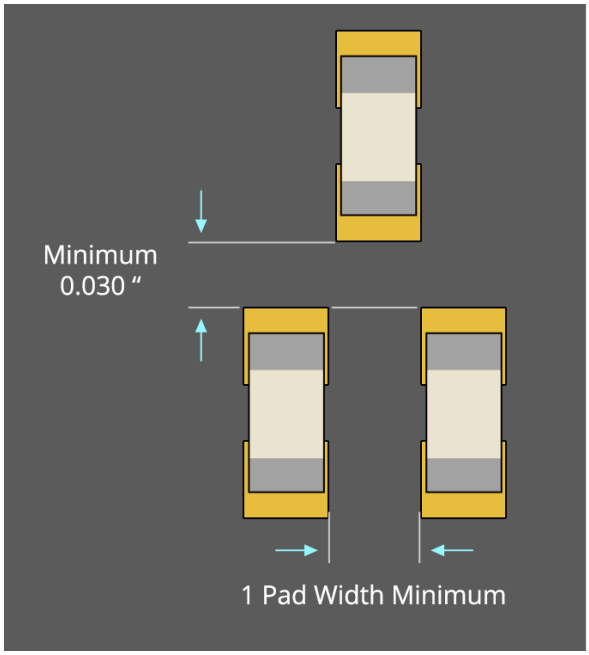
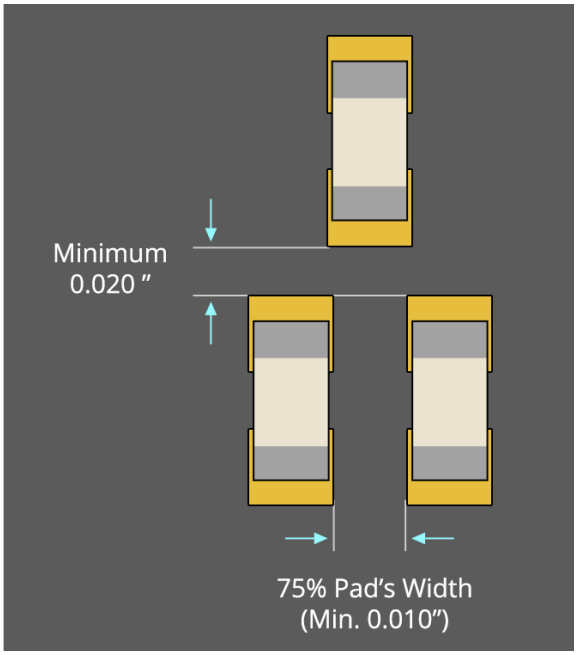


Figure 30 - Component Spacing to Avoid Shadowing and Unsoldered Termination

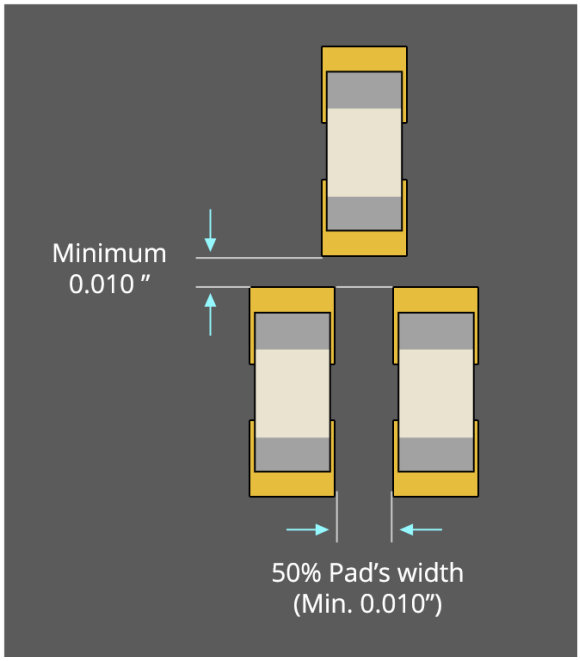
It is recommended that component-to-component spacing be 1x the component height (or a minimum of ½ its height). Figure 31 a nd b shows the minimum recommended component spacing for some of the most common package types. For a more detailed on component spacing please refer to IPC-7351[4-1].



Manufacturable



Less Manufacturable



Difficult Manufacturable

Figure 31a - Recommended Minimum Spacing Between SMD Components Based on SMT Density

Component-to-Component Spacing

ALL DIMENTIONS IN MILS

From \ To	Chip	Tantalum	SOIC	QFP/QFN	SOT23	PLCC	BGA	CSP	DIP
Chip	40	50	40	100	50	50	125	125	60
Tantalum	50	50	55	100	75	100	125	100	60
SOIC	40	55	50	100	50	100	125	125	60
QFP/QFN	100	100	100	100	100	100	250	250	100
SOT23	50	75	50	100	35	100	125	125	60
PLCC	50	100	100	100	100	100	125	125	60
BGA	125	125	125	250	125	125	250	250	125
CSP	125	100	125	250	125	125	250	100	125
DIP	60	60	60	100	60	60	125	125	100

Figure 31b - Standard Clearance Requirements for Component Spacing Based on Type[4-2]

NOTE: Sockets (for PLCC and DIP) and connectors should be away from BGA and CSP components to prevent solder joint cracking due to possible stress exerted during second loading/removal of add-on cards or IC components.

(*) For primary side only. For secondary side 0.125" clearance for all SMT components from DIP pins requiring selective wave solder fixture. Press fit connectors are an exception and do not require this clearance on the secondary side.

(**) Advanced Option if absolutely necessary:
0402 components can be 20 mils apart.
0603 components can be 25 mils apart.
These numbers applies to Viasystems only and requires special setupon their side.
Viasystems should be notified before the board is built.

Component and Board Orientation

It is important to spend time carefully orienting your components as it directly affects your board manufacturability and the reliability of the assembly process. A few variables will determine how your board will be placed and soldered through your manufacturer's assembly equipment, including the tooling holes, connector locations, edge components, and the PCB outline. See Figure 32 for a comparison between board layouts with poorly placed components and those with adequate spacing.

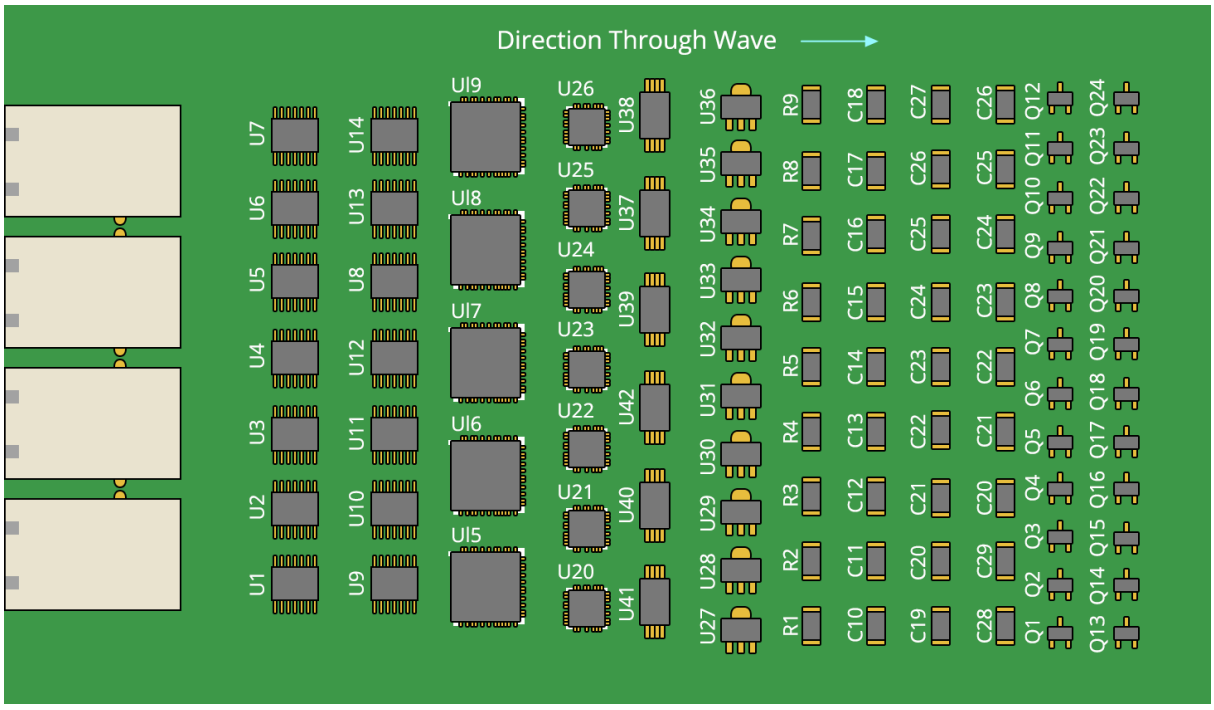


Figure 32a - Clustering Large components Requires High Temp Reflow (can damage Chips)

This board will have to be reflowed at higher temperature which could cause damage to chip components. This due to having large components located in one particular area of the board.

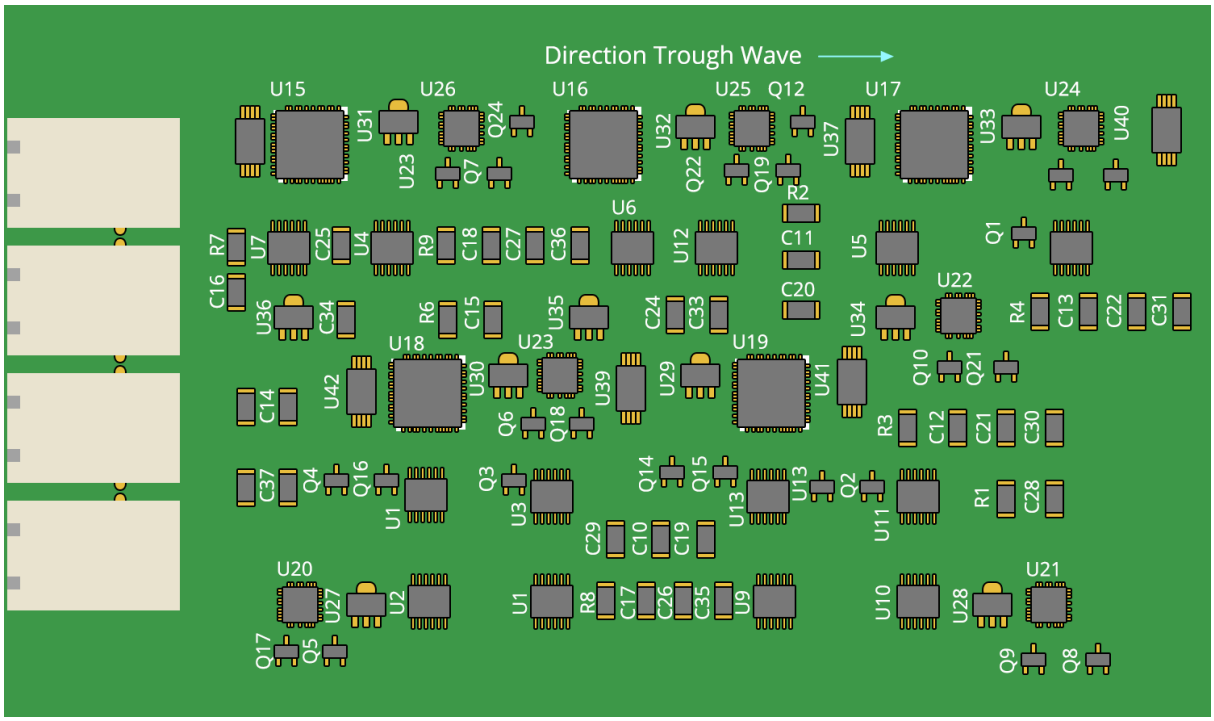


Figure 32b - Spreading Out Large Components for Better Thermal Distribution

For better thermal distribution it's best to spread out large components throughout the board.

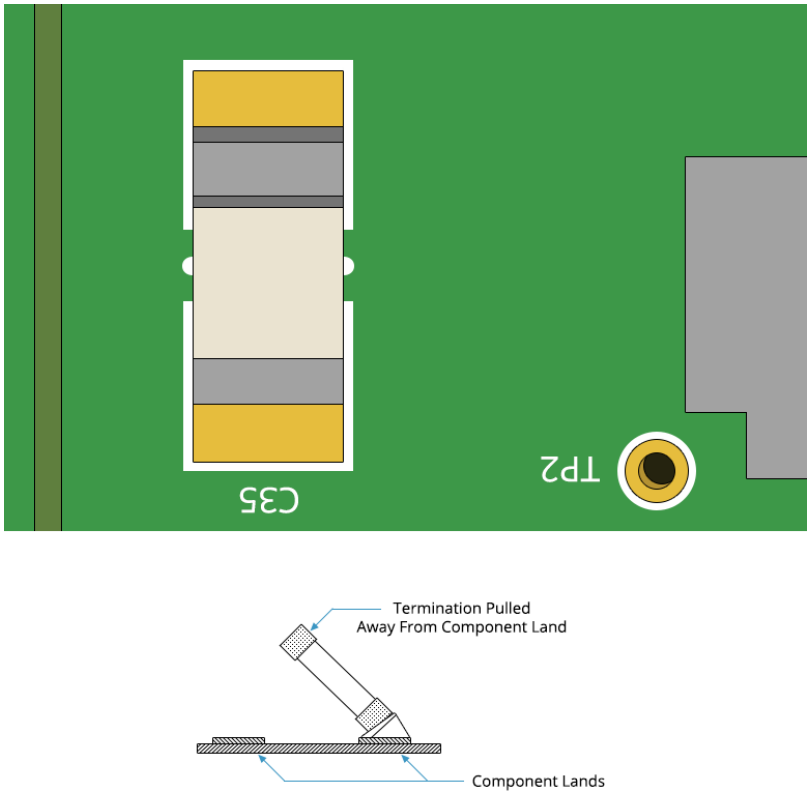


Figure 33: Termination Pulled Away from Component Pad Due to Poor Thermal Balance (Tombstoning)

If your board consists of large components with heights greater than 0.20” it is recommended to make the component-to-component spacing equal to the height of the largest component package. This strategy gives ample room for visual inspection and makes rework easier.

To achieve a better thermal balance of your board during reflow, you should distribute the components as evenly as possible throughout your board. This will ensure that no area on your board will be substantially hotter than another. It is also recommended to avoid concentrating large components in one area of your board to help minimize bow and twist while providing a balanced thermal distribution.

Board Orientation for Wave Soldering

Manufacturers typically prefer a board to be on its long axis when flowing through a soldering machine. This will minimize the setup complexity and prevent a board from bulging downward during soldering. See Figure 34 for an example showing a unpreferred board orientation dictated by the card edge connector, which would interfere with the gripping assembly if rotated to the preferred long axis.

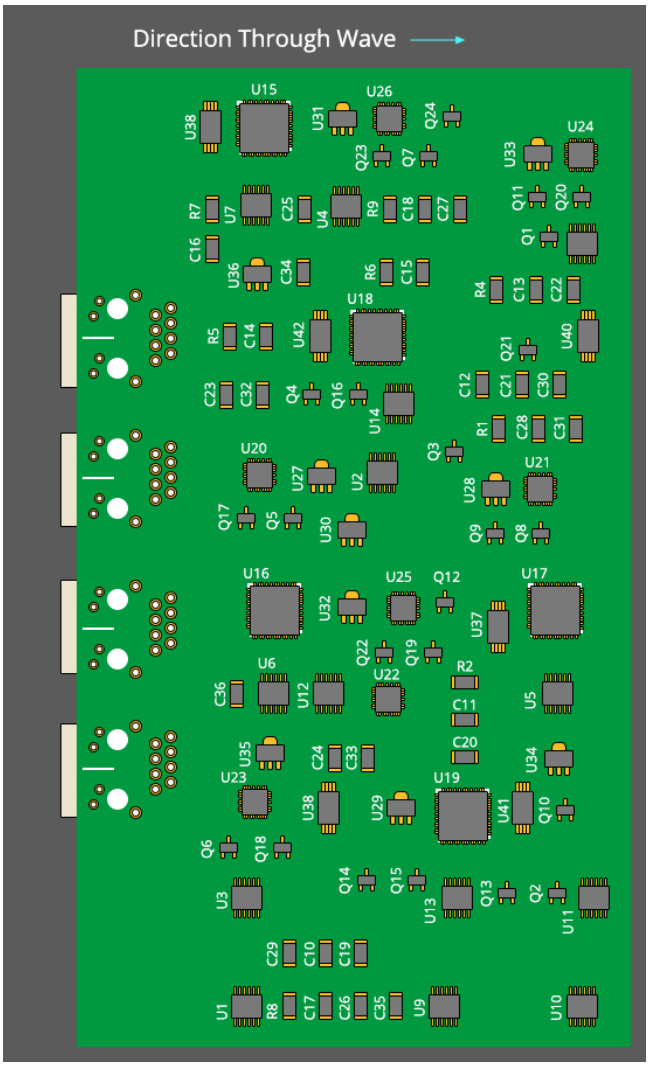


Figure 34 - Unpreferred Board-to-Solder Orientation

Component Orientation

The geographic location of a component on a PCB is important for proper board manufacturability. It is recommended to orient your components relative to your board outline and the solder process on the long axis of the PCB, where your small outline ICs (SOIC) are set in parallel to the solder flow direction as shown in Figures 35 a and b.

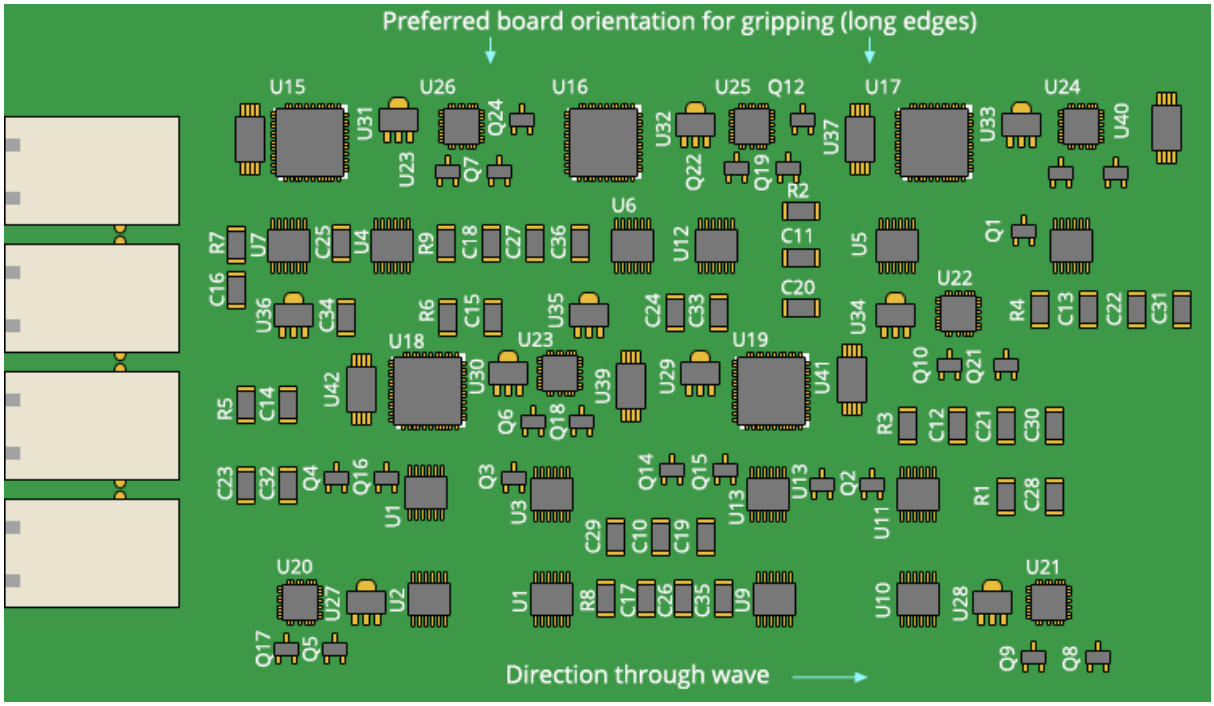


Figure 35a: Board in This Orientation (Top & Bottom) is Soldered in the Long Axis (Preferred Orientation)

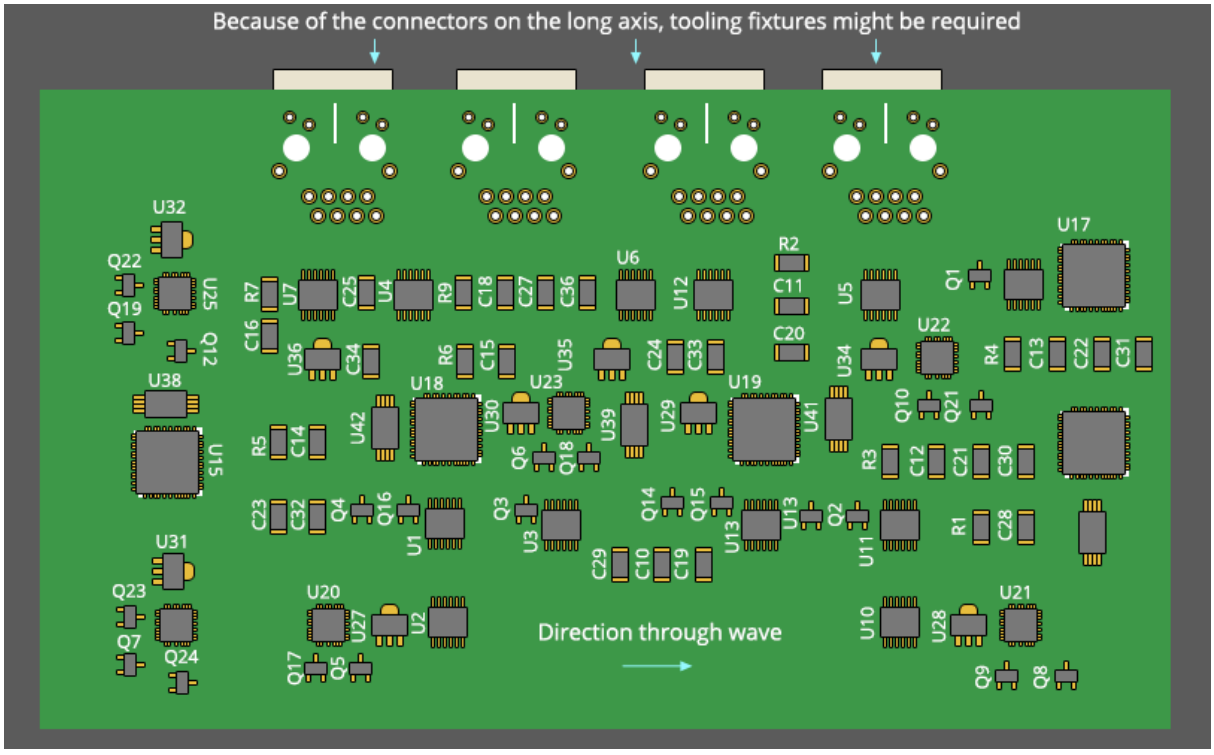


Figure 35b: Bottom Side Component Orientation for Wave Solder (Non-Preferred)

For chip components, both terminations should be parallel to the solder wave so they can be soldered at the same time. Avoid shadowing by not placing chip components perpendicular to each other. This will also help to avoid uneven solder fillets (and skips) that usually put stress on solder joints. Figure 36 shows a visual example of correct chip component orientation.

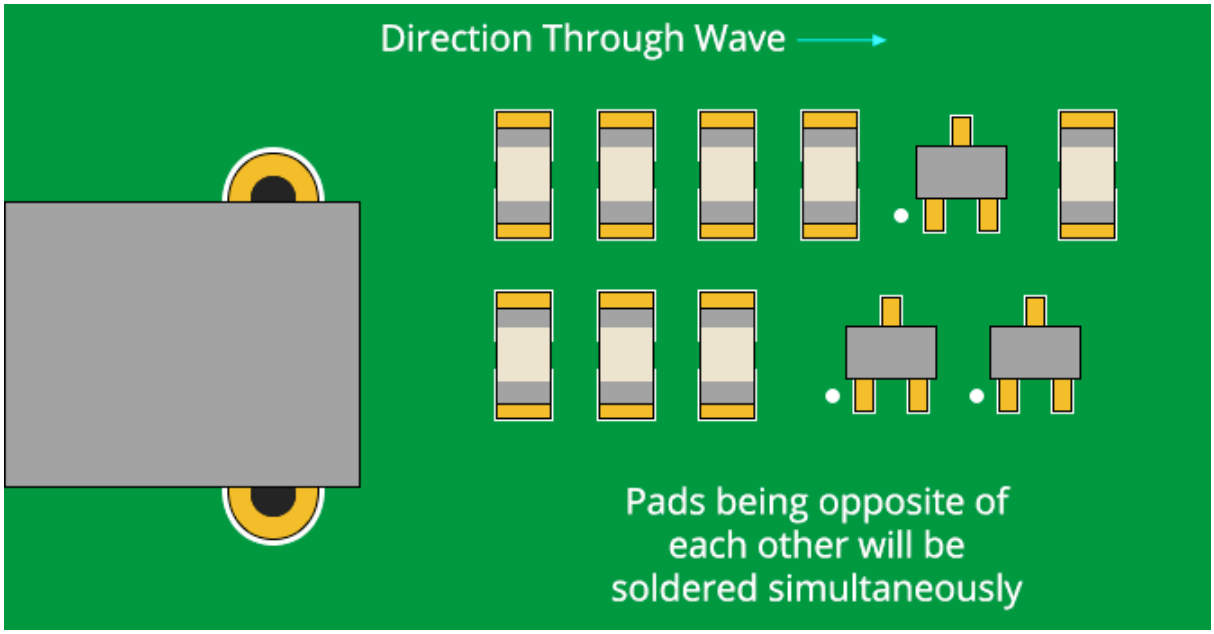


Figure 36a: Good Chip Component Orientation

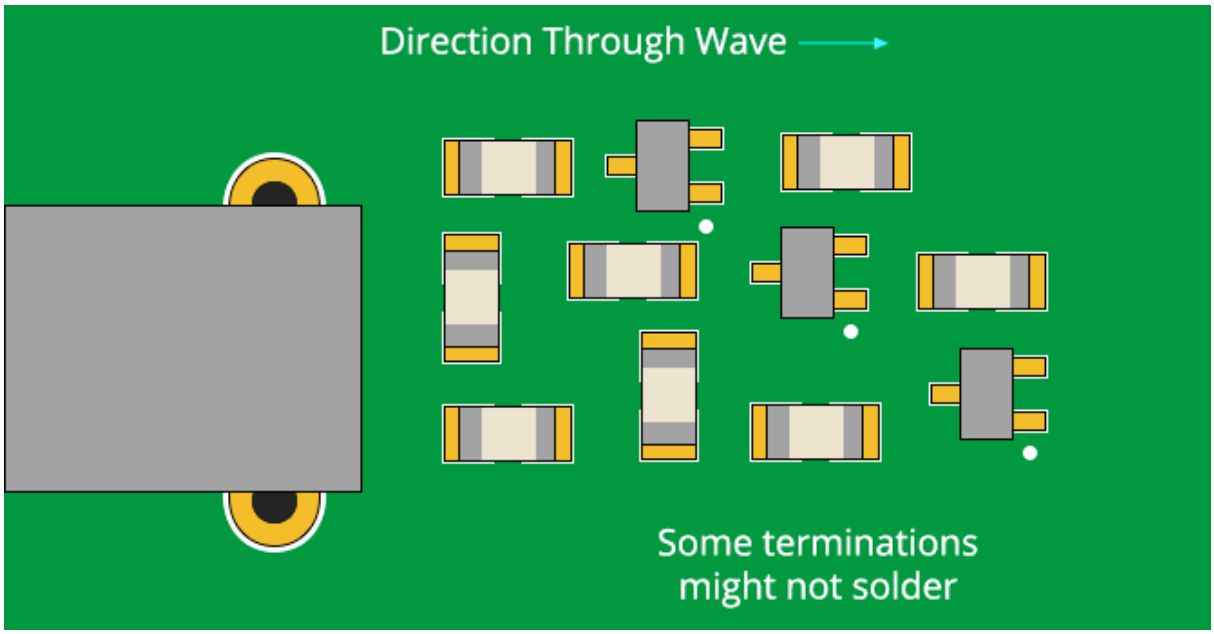


Figure 36b: Poor Chip Component Orientation

The more shadowing of smaller components you have on your board from the solder wave, the more likely your PCB will end up with open solder joints. Ensure that the soldering direction of your board is positioned in a way that large components will not shadow the smaller chip components as shown in Figure 37 below.

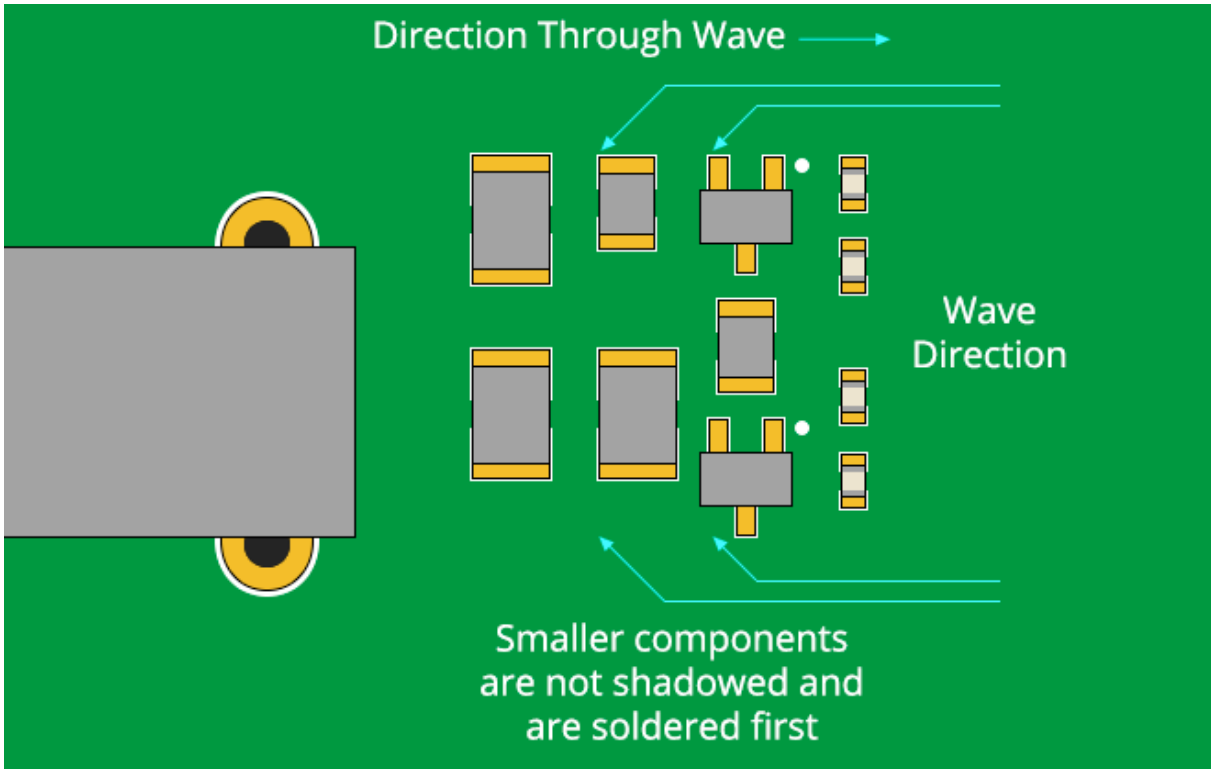


Figure 37a: Good Component Placement

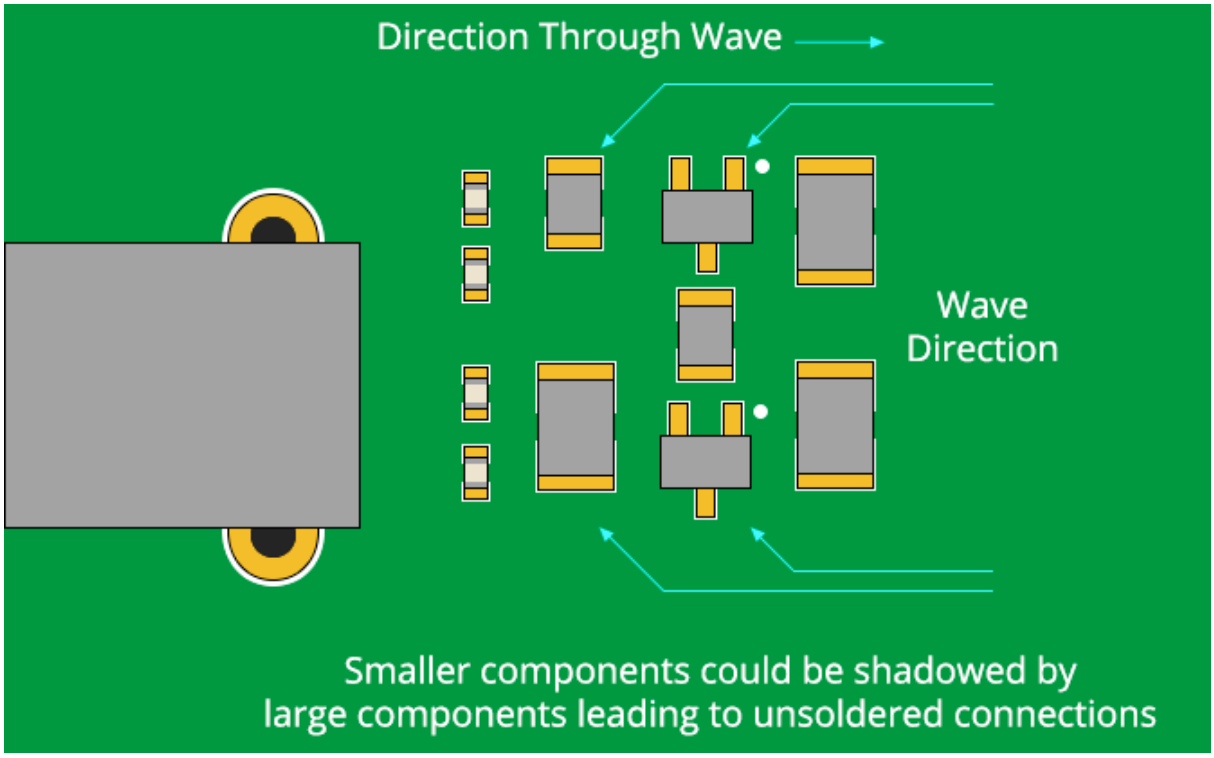


Figure 37b: Poor Component Placement (Shadowing)

BGA Orientation

It is recommended to place BGAs on the top of the board to eliminate the possibility of open solder connections during the second pass reflow. Your manufacturer might require additional steps in the assembly process if you have BGA components on both sides of your board.
These additional steps will ensure a temporary support to the other side of a BGA during the second pass reflow process.

Avoid placing BGA and larger quad flat package (QFP) components in the center of the PCB to prevent board warpage caused by heavier parts. Not following this guideline can result in open solder connections as shown in Figure 38, and is a concern for standard 0.062” boards when the board area is greater than 25 square inches.

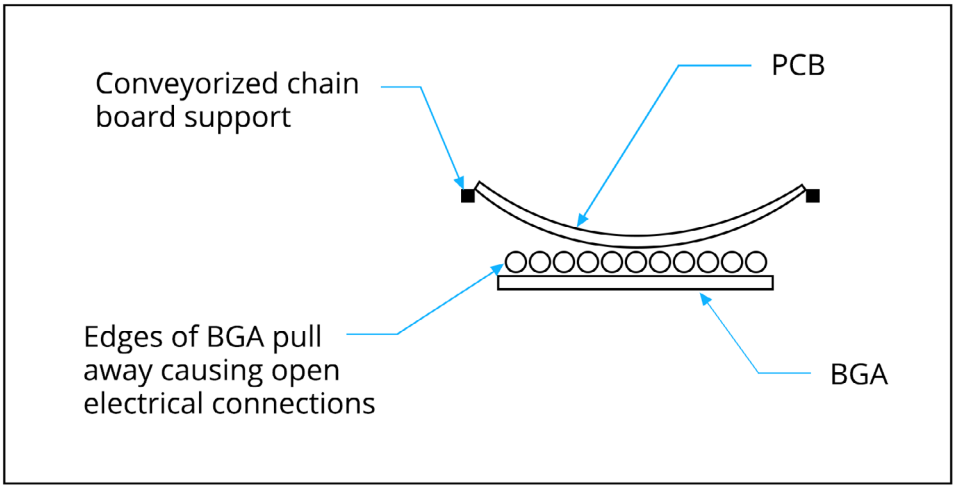


Figure 38 - Example of the Bow-and-Twist Effect on BGA Devices

If your design has BGA components on both sides of the board, it is recommended to offset each BGA to ease rework and facilitate the solder ball inspection as shown in Figure 39.

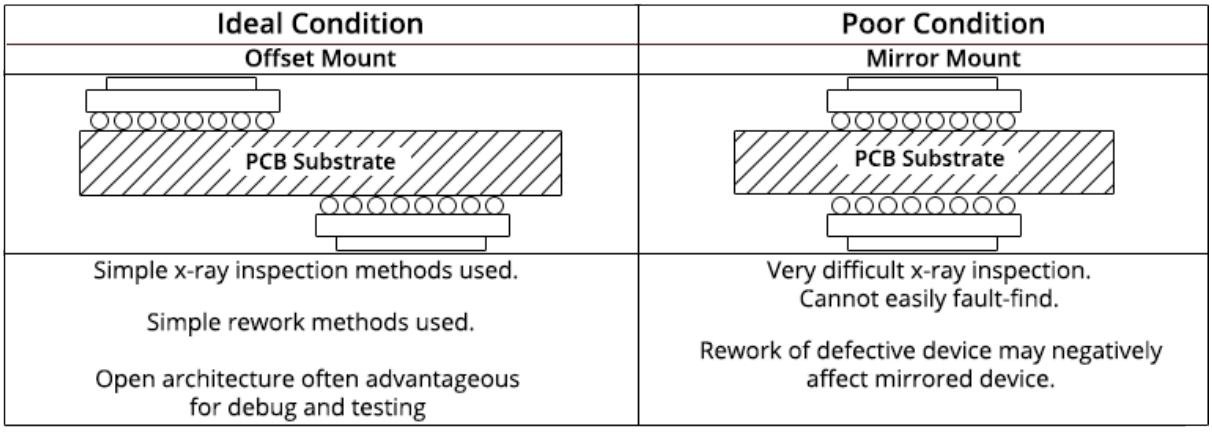


Figure 39 - BGA Mounting Strategy

Chip Under Device Placement

When you specify a chip under a device, this can make inspections, rework, and test more difficult. If placed under BGA sockets or ZIF sockets, you will need to account for the BGA ball collapse, which is typically around 25% of the ball diameter. It is recommended to keep the stackup tolerances in mind with these type of designs as they make it impossible to inspect hidden devices and make it challenging to perform rework.

Resistor Pack (R-Pack) Placement Limitations

Resistor packs with convex-type termination and external solder joints are preferred by PCB manufacturers. These types of resistor packs have better spacing and easier termination soldering, which makes the visual checking and inspection of the solder joints easier.

Capacitor Placement

To keep your design consistent and assist with the assembly process, it is recommended to place all polarized capacitors in an orientation where the positive end is to the right or down. As you saw earlier, the polarity should be indicated on the silkscreen on the package outline. Decoupling capacitors should always be placed as close as you can get to them to the IC's power pin and oriented perpendicular to SOIC components and the solder flow.

Double-Sided Boards

The spacing between pads (land-to-land) that are perpendicular and parallel to the solder direction should be at least 0.025" to avoid solder bridging. It is also recommended to maintain a minimum of 0.025" spacing from a through-hole pad or via edge to a surface mount pad or another via.

Components and Wave Soldering

All components used on the wave solder sides of an assembly should first be approved by your manufacturer for immersion in a solder bath. For tall components (taller than 0.0100") such as tantalum capacitors, it is recommended to have at least 0.100" land-to-land clearance (from all directions) to avoid skips and open connections during the wave solder operation.

Some types of components are sensitive to wave soldering at higher temperatures, and it is not recommended to place them on the backside of your board (bottom layer) where the solder wave would contact the component. Components that are not recommended for placement on the backside of a board (bottom layer) include:

- BGA components.
- Non-encapsulated inductors.
- QFP components.
- “J” leaded devices.
- Connectors.
- Any other device that cannot be submerged in solder.

Through-hole Components

When determining your required PTH finished size, keep in mind that if the PTH is too large, the component will not stay in place and could misalign, increasing the “lift” probability and creating shorts due to solder flooding during wave soldering. If the PTH is too small, the component might not fit in the PTH and could result in insufficient solder fill. It is easy to disorient a through-hole component, so directional packages are preferred over bi-directional ones. Figure 40 gives a general set of guidelines to determine PTH finished sizes:

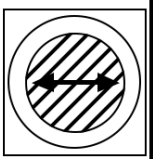
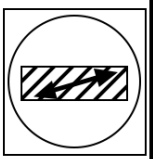
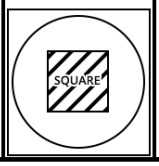
				More Manufacturable → Less Manufacturable			
				Lead Clearance	Lead Clearance	Lead Clearance	Lead Fee
	Configuration	Measure	Condition	A	B	C	Recommendations
Round Lead			Max. Hole to Min. Lead	No greater than 32 mils	No greater than 28 mils	No greater than 24 mils	Increase nominal hole size by 10% or 2 mils (which ever is greater)
			Min. Hole to Max. Lead	No less than 10 mils	No less than 8 mils	No less than 6 mils	
Ribbon Lead			Max. Hole to Min. Lead	No greater than 10 mils	No greater than 8 mils	No greater than 6 mils	No Change
			Min. Hole to Max. Lead	No less than 5 mils	No less than 4 mils	No less than 3 mils	
Square Lead			Max. Hole to Min. Lead	No greater than 20 mils	No greater than 16 mils	No greater than 12 mils	Increase nominal hole size by 10 or 2 miles (which ever is greater)
			Min. Hole to Max. Lead	No less than 5 mils	No less than 3 mils	No less than 2 mils	

Figure 40 - Pin-to-Hole Recommendations for Through-hole Components[4-3]

With the information presented in this chapter, you are now well-equipped to begin your component placement and orientation process to meet fundamental manufacturability requirements. Before beginning your component placement process, it is recommended to consult with your manufacturer to discuss any specific placement requirements that were not outlined in the sections above. Now that your design is well on its way to completion, it is time to finalize the board layout process by configuring your test point requirements in the next chapter.

Configuring Your Test Point Requirements

Defining proper test points on a board layout during your design process is critical for having your PCB tested and verified by your manufacturer. The test points you establish will ultimately determine the reliability of your PCB, and will allow your manufacturer to identify and diagnose any potential issues before your board ever leaves the processing facility. This chapter will cover general testing requirements for your PCB, and will then go into the specifics of test pad placement and panelization.

General Test Point Requirements

Before going into the specifics of test point and pad requirements, there are several general guidelines to keep in mind:

- Each node on your board should have at least one test probe point (preferably two), including the component pins connecting to that node.
- It is not recommended to use component leads as test points as this method can result in missing and cracked solder joints.
- It is recommended to spread your test points throughout your board, rather than have them concentrated in any one board location as this will help to avoid air leaks in the vacuum sealing process of your packaged board.

Test Pads

Test pads can be either vias/pads, a component pad (PTH), or a specified Test Point (TP) with its own reference designator.
See Figure 41 for an example of a through hole test via.

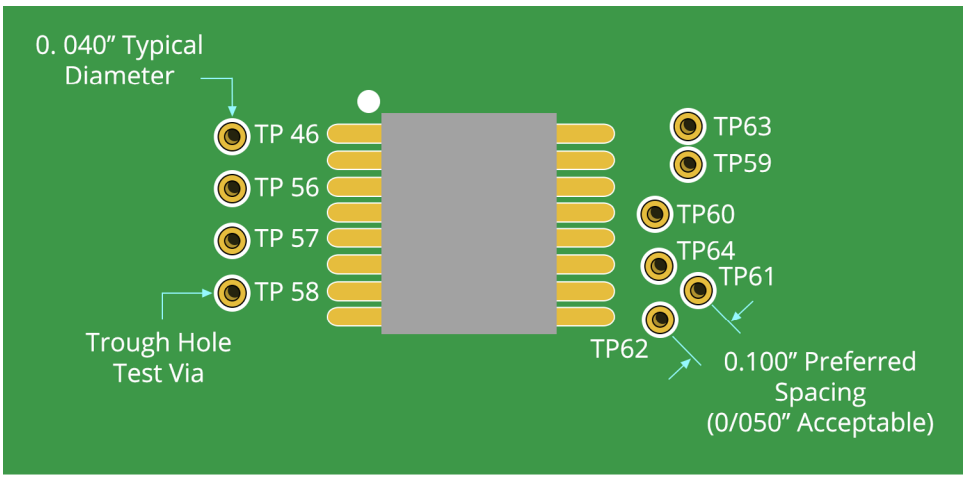


Figure 41 - Through-hole Test Via

For test probes, use the test pad diameters below to ensure proper testing results during your manufacturing process:

- For standard 0.100”, 0.070” or 0.050” test probes, test pads diameter should be between 0.015” and 0.040” and they should have enough solder surface for a reliable probe contact.
- If your design requires the use of 0.030” to 0.015” probes (e.g. fine pitch devices), test pads should have adequate spacing around them (no less than 0.050”).
- The 0.030” to 0.015” probes are more fragile, more expensive, less reliable, and their use should be minimized.
- For larger boards (more than 12” on either side), keep the test pad size to a minimum of 0.040”.
- In general, test probe pads should not reside within at least 0.125” of board edge.

Test Pad Spacing and Tooling Requirements

The spacing between test pads (center-to-center) should be maintained at 0.100”. This will enable the use of larger probes which are less expensive to setup and provide a more reliable reading.
The smaller the spacing between the test pads, the more likely your manufacturer will have to use smaller, costlier, and less reliable probes as shown in Figure 42.

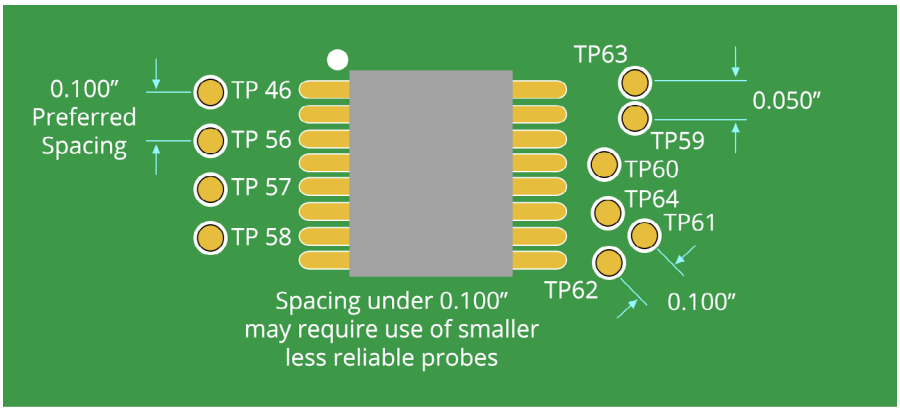


Figure 42 - Test Pad Spacing

Test Pads for SMT Boards

Components on SMT boards that are 0.35” high (or more) are difficult to probe, so it is recommended to keep the clearance at 0.100” between the test pads and the edge of these components. This will prevent requiring cutouts or relief in the probe plate if the pad-to-component spacing falls below the required minimum as shown in Figure 43.

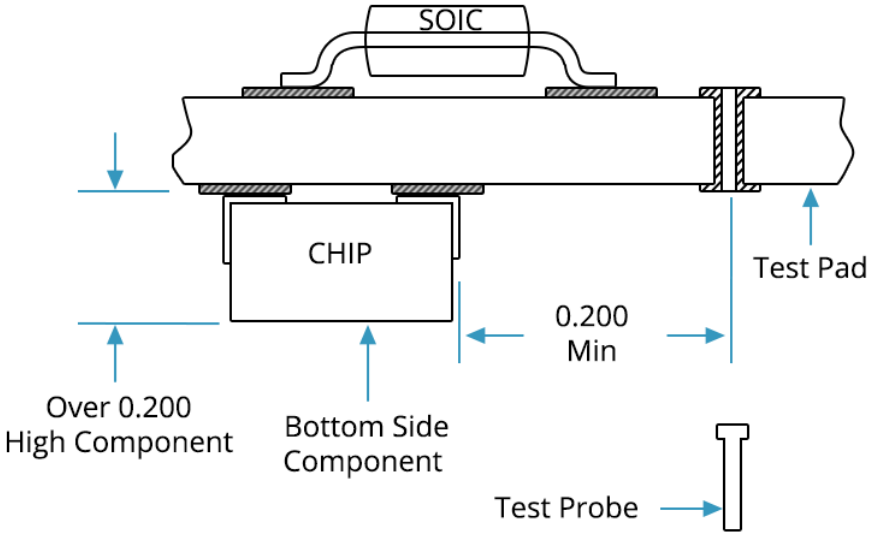


Figure 43 - Test Pad to Component Spacing for Components Over .200” high

For components less than 0.35” high, test pads should be placed at no less than 0.040” away from the component edge.
This will avoid damaging either the probe or the component due to tolerances in component placement and fixturing as shown in Figure 44 .

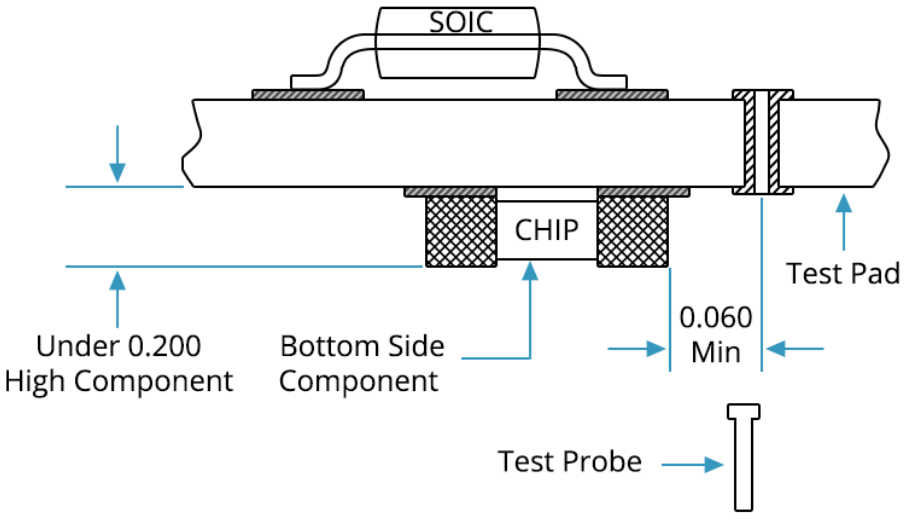


Figure 44 - Test Pad to Component Spacing for Components Under 0.200” Height

Test Tooling Requirements

At a minimum, two tooling holes are required on the PCB. They should be as far apart as possible, diagonally placed, and have a 0.125” diameter. The free zone area around the tooling holes should have a 0.125" annular radius.

Panelization

Panelization, also known as step-and-repeat, is the method of placing two or more PCBs onto one panel, which allows boards to be secured during manufacturing, shipping, and assembly. Since your PCB is priced per panel, your cost will be directly impacted by how many PCBs can be fabricated on a panel. Panelization can also save you time by processing multiple boards at once in bulk as shown in Figure 45.

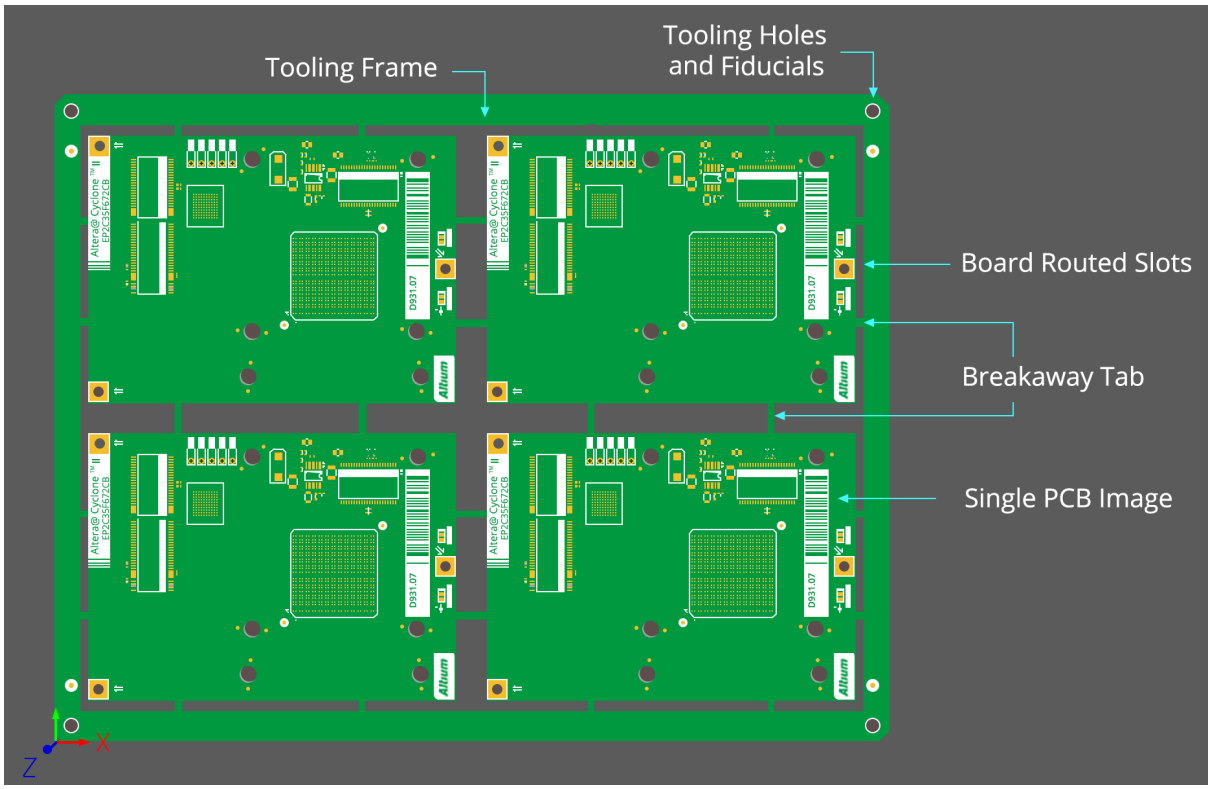


Figure 45 - Rectangular Circuits in a Single Panel with Tooling Holes and Breakout Tabs

The PCB images on a panel can be a single design or a grouping of various designs. A number of holes are drilled at several locations along the edge of the panel, with the board outline not completely routed to make a tab. Once on the panel, boards can then be easily snapped out before or after being populated with components.

It is recommended to consult with your manufacturer to determine whether panelization is required to have your board manufactured.
The factors that will govern how many PCBs can be fit onto one panel include:

- Size of the individual design.

- Total weight of placed components.
- Assembly Equipment Panel Size.
- Extra clearance needed for overhanging components.

As the number of circuits increases within a panel, its mechanical strength becomes weaker and can cause the panel to bend under its weight during assembly and reflow. While a smaller panel containing fewer boards could be stronger, it may not be the most efficient way to utilize the PCB manufacturer's standard fabrication panel sizes and will add additional costs during the assembly process.

General Guidelines for Panels

The average panel is approximately the size of an A4 sheet of paper. The following specifications should be included for a standard panelization:

- Breakaway strips should measure around 0.400" .
- Fiducials should be at least 0.125" away from a card edge.
  or panel frame edge
- Panel designs should have 0.125" un-plated tooling holes located 0.2" from.
  frame corners (or per your manufacturer's guidelines)
- A panel design drawing that includes:
  - Panel dimensions length and width.
  - Breakaway rail dimensions.
  - Fiducial target dimensions and locations.
  - Tooling hole dimensions and locations.

Tooling Strips

Since a PCB needs to be held in place by assembly equipment, there is usually a need for a component free area of 0.200" on both sides of the board. If components are closer than this, a tooling strip will be needed, and an additional 0.400" of waste area will be required around the board edges. If your design happens to have components overhanging the PCB edges, the tooling frame width should be increased accordingly. Although not required, having a 0.100" chamfer on the tooling bars corner will make it easier for the assembly equipment to align with the board and will help to avoid any jamming risks. Figure 45 shows a standard panel with the tooling strips, holes, and frames included.

The tooling strips are discarded after the assembly is complete and the individual circuits are removed. If your design doesn't contain any overhanging components, and the closest component to edge is at least 0.100' away, the tooling strips along the top and bottom edges will be included as shown in Figure 47 below:

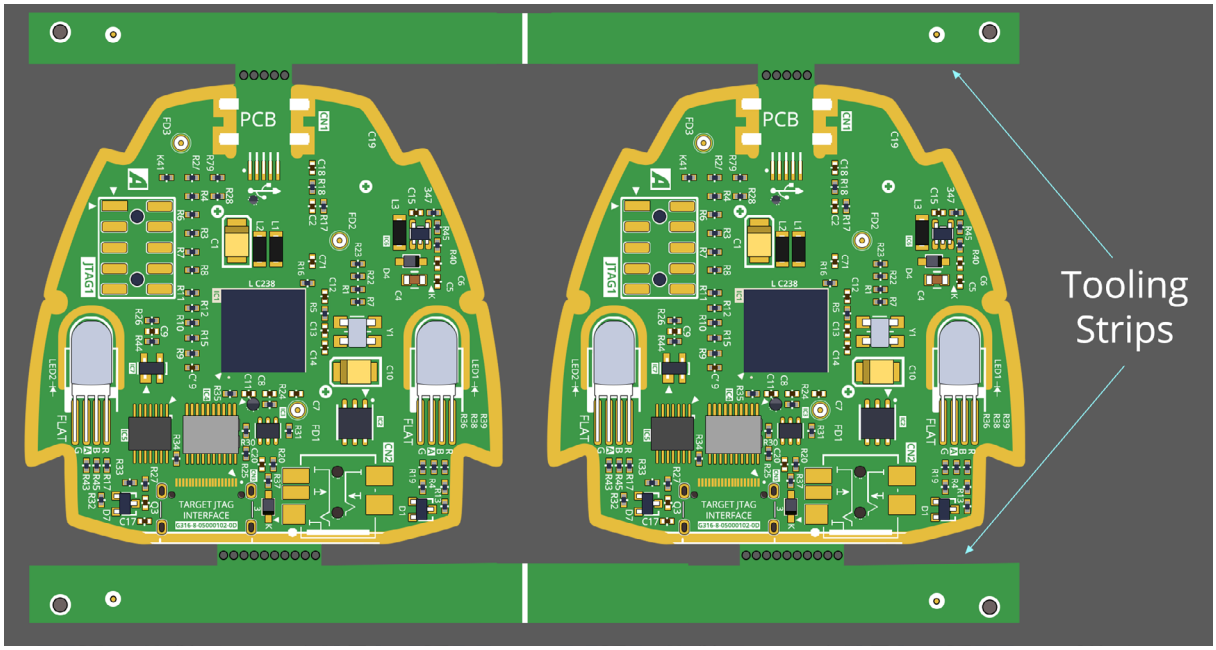


Figure 47 - Tooling Strips Along the Top and Bottom Edges of a PCB

Tooling Holes

Tooling holes are required to accurately align and position the circuit board in machines and fixtures to be processed (e.g. routing fixtures, solder paste screen printing process, drill machines, test fixtures, etc.). The minimal configuration should include at least two unplated holes, one in each corner (opposite of each other), with 0.125" diameter and 0.200” away from the edge of the board. A third hole is desirable, if space allows, as it will improve the alignment accuracy and can be used to ensure the board will not be placed in the fixture in the wrong orientation.

Due to the auto placement insertion heads limitation and the tooling contacts, a component-free zone of about 0.400” from the center of the hole should be maintained. These requirements can vary depending on the insertion machine so it is recommended to consult with your PCB manufacturer to ensure the best configuration. Proper placement of tooling holes can be seen in Figure 48:

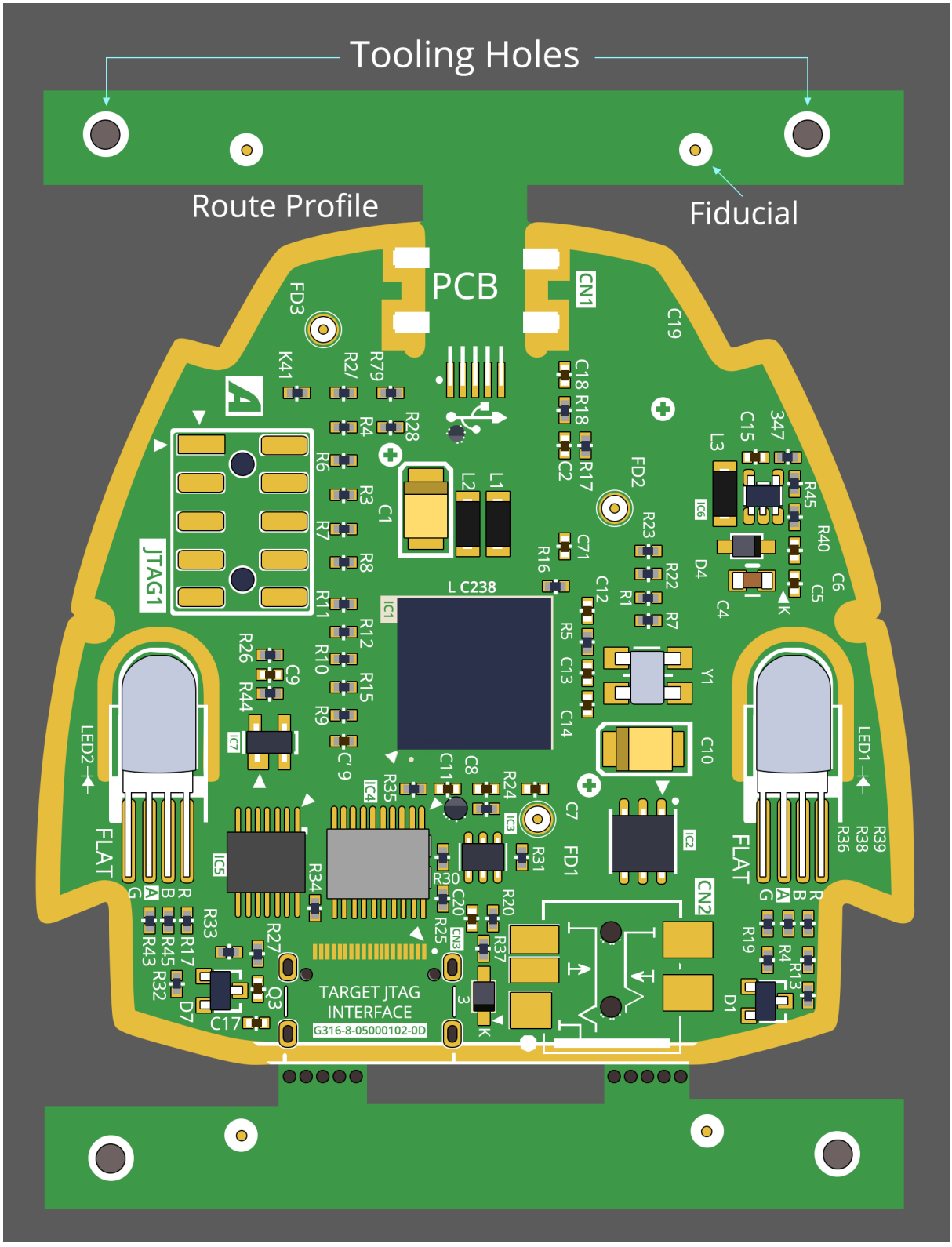


Figure 48 - Proper Tooling Hole Placement on a PCB

Depanelization Process

There are several depanelization methods outlined below, all of which have their benefits for use depending on the physical constraints of your board shape and associated components. Your specific design requirements will determine what particular depanelization process to use, and it is recommended to consult with your manufacturer to select the ideal solution.

Breakaway Tabs

To support the individual PCBs during the assembly process and be able to remove them once the assembly is complete, several small breakaway tabs are added around the perimeter of the PCB profile.

For better stability, at least two tabs are required at each edge of your board. These tabs should be non-plated through-holes between 20 mils and 30 mils in diameter and spaced between 40 mils to 50 mils as shown in Figure 49. This method has the advantage of being easy to break off the board from the panel, but will leave a rough edge. If you have tight tolerances for a mechanical enclosure, the holes can be offset into the PCB to eliminate any material beyond the PCB edge.

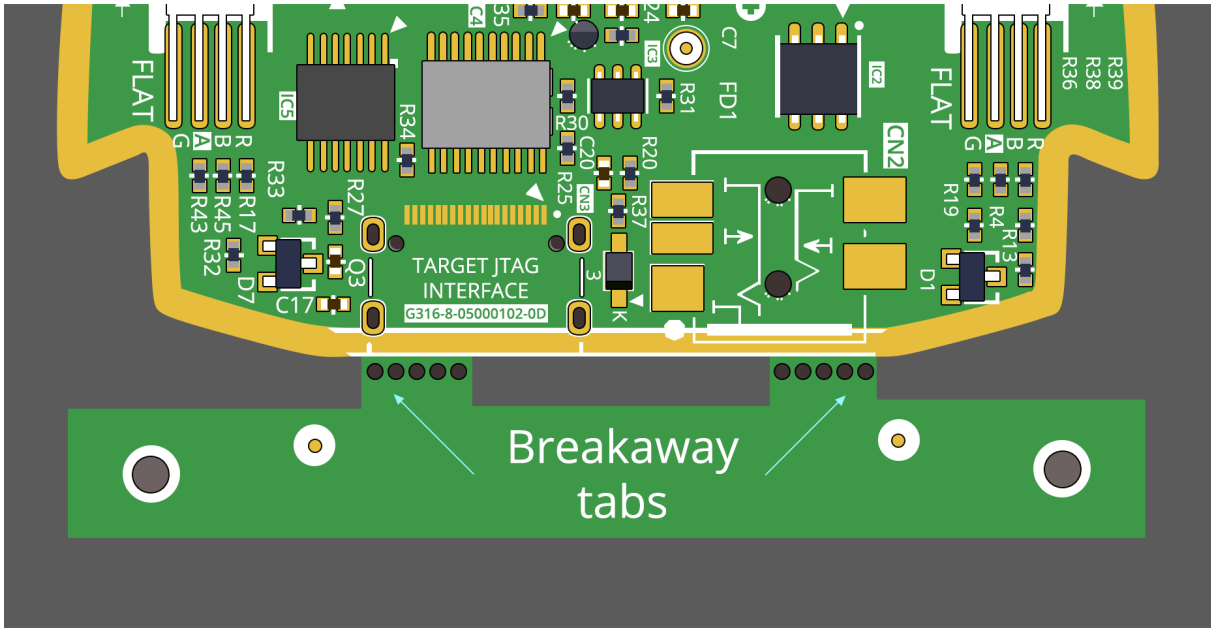


Figure 49 - Breakaway Tabs

During breakout some stress will be placed on the laminate and SMT components positioned near the tabs can be damaged. To minimize the damage, it is recommended to orient these components 90° to the board's edge. In general, components, tracks, vias and inner layer planes should not reside within 0.100" of breakaway holes.

Solid Breakaway

The solid breakaway method is stronger and uses less material than breakaway tabs, and also doesn't require a nibbler to remove a board from a panel. After the PCB is broken out, the board tends to leave a bit of unwanted material on its edge, which might require some filling to level the board. Figure 50 shows a solid breakaway cross section on a PCB:

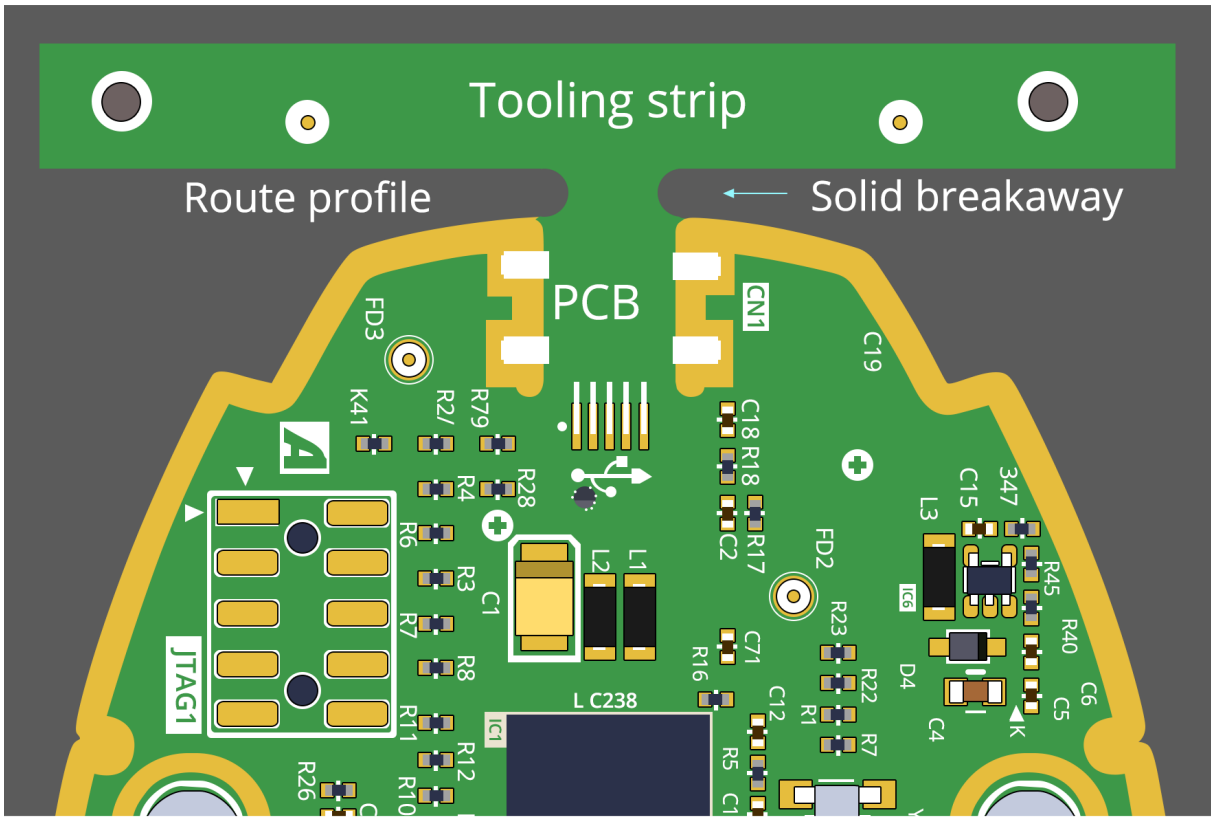


Figure 50 - Solid Breakout Pip

V Grooving

V grooving, or V scoring, is another alternative to break away boards from the panel, and it is often a good option for boards without any overhanging components. This alternate depanelization method costs less to implement and is ideal for volume production. A cross-section of the V grooving method is shown in Figure 5:

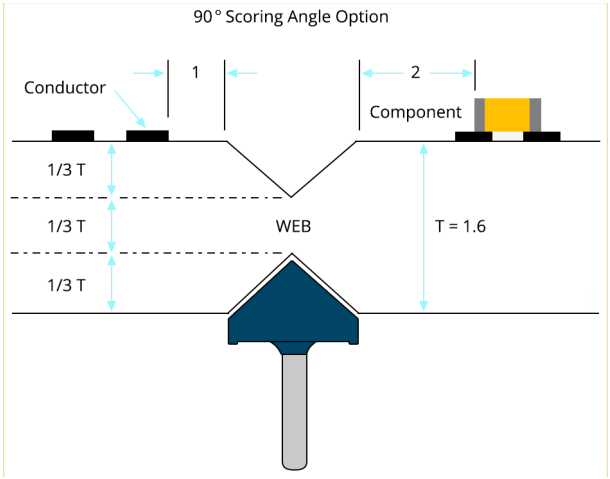
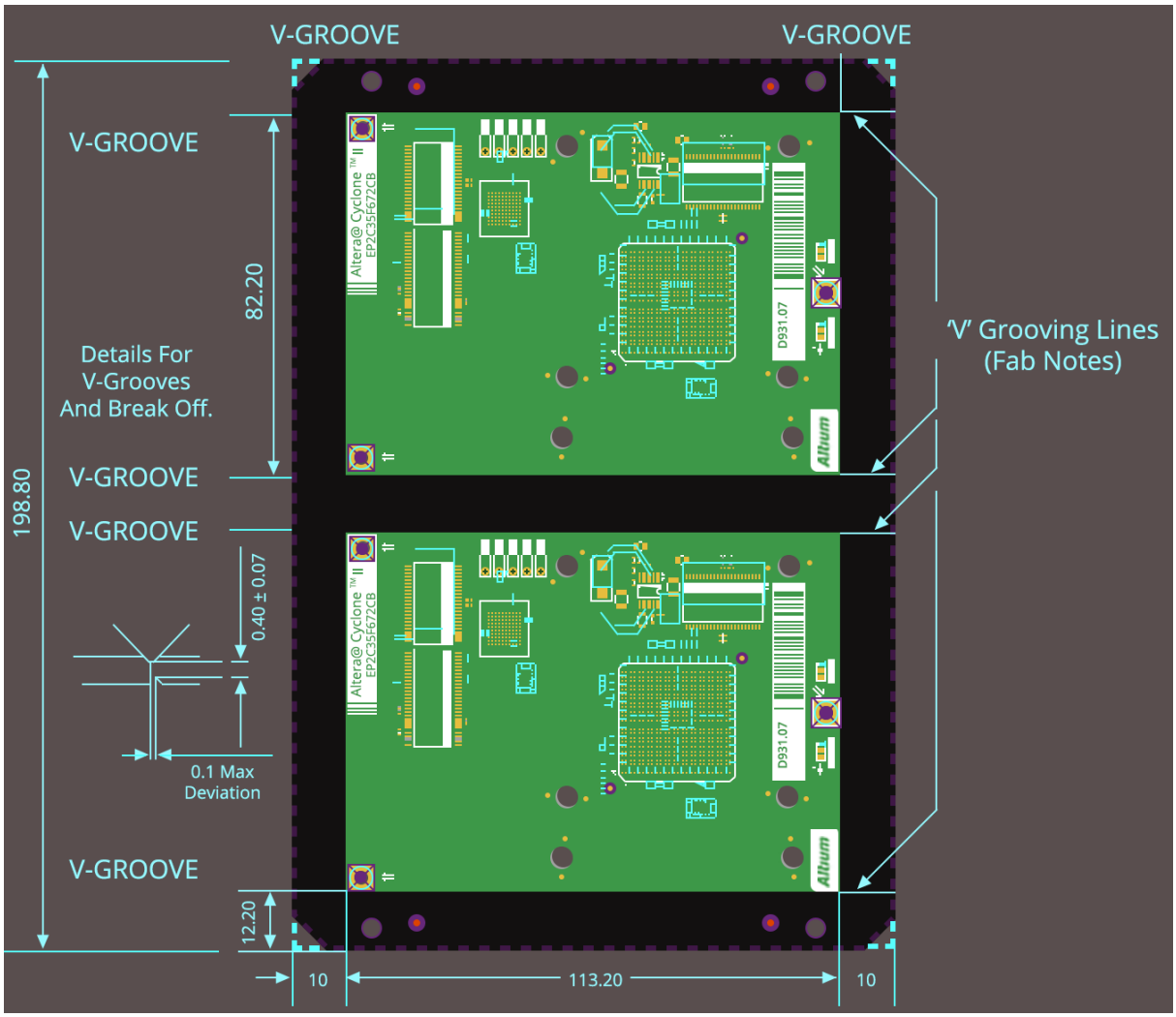


Figure 51a - V Groove Cross Section

Breaking away boards from the panel using V grooving will create some stress along the area being snapped, so it is recommended that SMT components are placed no less than 0.100” from your board edge. V grooving will also produce a rough, unfinished board edge after it is scored by your PCB manufacturer. Figure 51b shows the required grooving lines on a panel for the V grooving method:



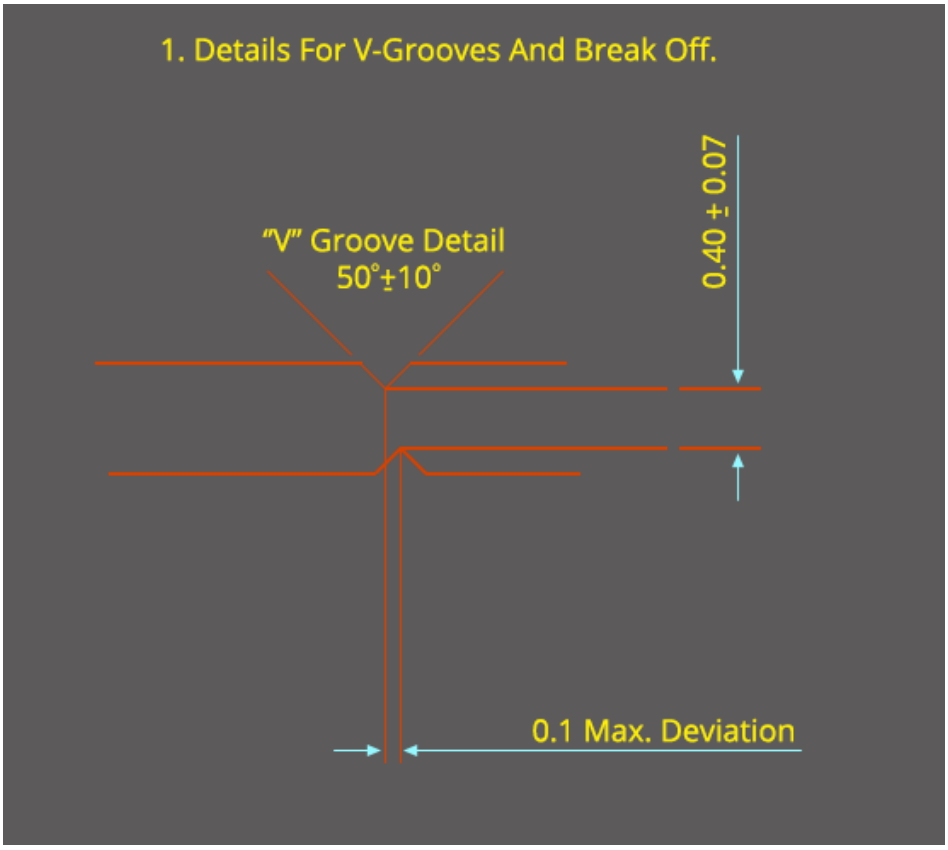


Figure 51b - Required Grooving Lines and Details on V Grooved Panel

Irregularly Shaped PCBs

If you are designing a PCB with an irregular shape, then it is recommended to utilize the panelization technique during the assembly process to streamline the production process for your board.
This will provide some material waste pieces as shown in Figure 52:

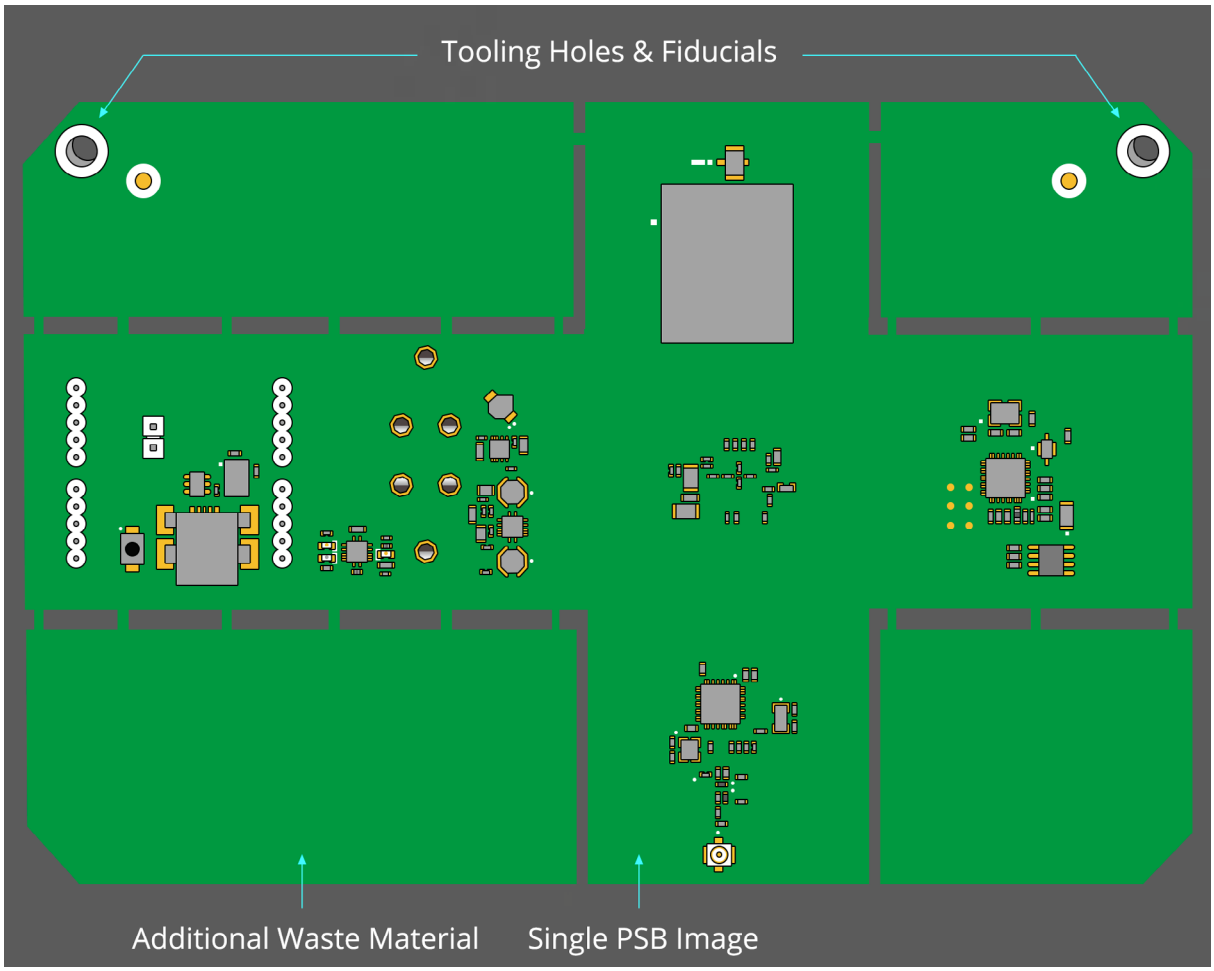


Figure 52 - Irregular Board with Infill Panels

Finalizing Your Board Layout

By adding proper test points on a board, you will significantly increase the likelihood of detecting any manufacturing related errors during the post-production validation process. Given that every design has its limitations and unique physical constraints, it is always recommended to consult with your manufacturer to determine the ideal placement of test points. With the layout process of your board fully complete, it is now time to move on to the post-design documentation process to clearly communicate design intent to your chosen manufacturer.

Documenting Your PCB For Fabrication

Before you can send your design off to manufacturing, you will need to ensure that it is properly documented to clearly communicate your design intent. While electronic files such as Gerber and ODB++ provide enough basic information to make your board, they don't include all of the fine details in your head about how you intend to have your board produced.

The documentation stage is your chance to precisely document your board layout and avoid any of design intent miscommunications that typically occur when design goals are not clearly conveyed. This chapter will focus on creating a standard PCB documentation template and outlines all of the necessary details you will want to include to increase understanding by your manufacturer. The following chapter will then go into the specifics of your master drawing. This, and the following chapter pull information from the standard, IPC-D-325A[6-1].

Drawing Sizes

The first step to create a master drawing is selecting an appropriate drawing area to contain all of your drawings.The dimensions of your drawing area are referred to as the drawing size and should comply with the ANSI-Y 14.1[6-1] standard sizes as shown in Figure 53[6-2]. If possible drawing sizes should be kept consistent for all documentation while still adhering to your company's documentation policies.

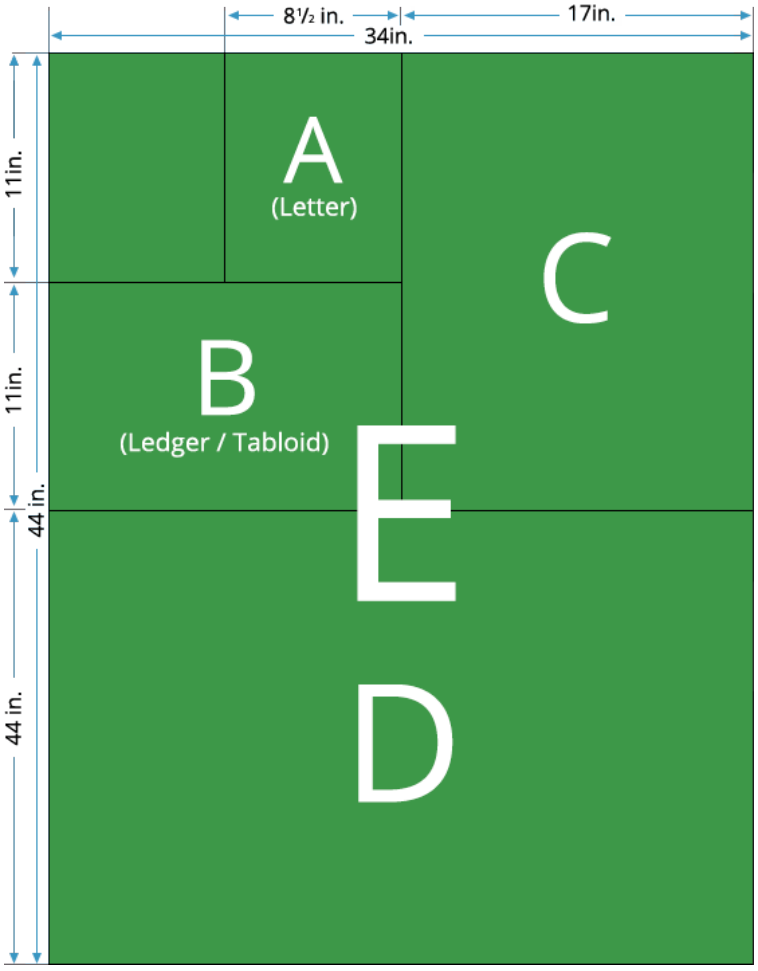


Figure 53 - Standard Drawing Sizes for PCB Documentation

Primary Blocks of a PCB Template for Fabrication and Assembly

There are several blocks that need to be included on your PCB drawing. A block includes additional details and specifications that will help to clearly define your design requirements for manufacturing and should be fully detailed to avoid any potential production delays or errors. Figure 54 shows a blank drawing space with the blocks highlighted.

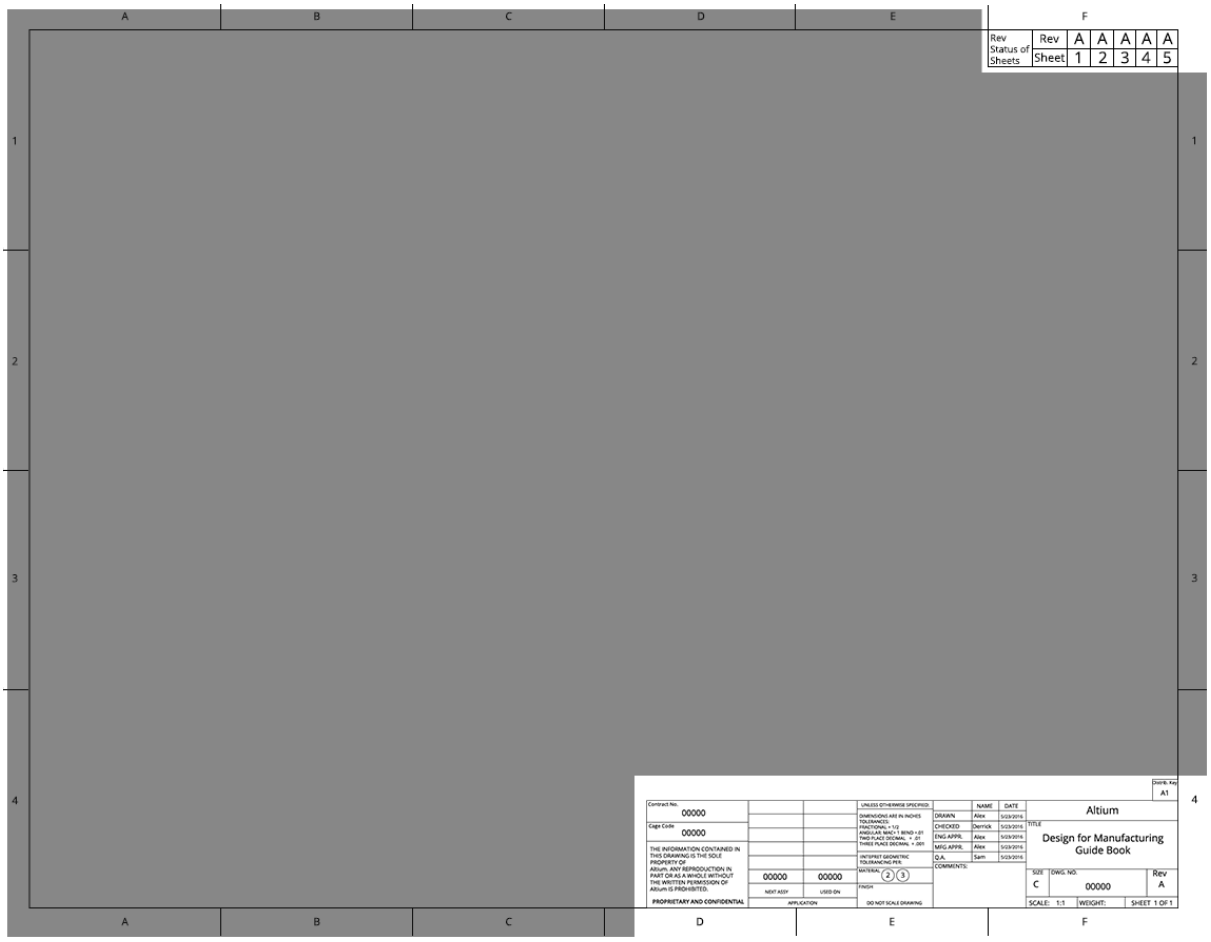


Figure 54 - Blank PCB Drawing Space with Highlighted Blocks

Zoning

Zoning is used to provide reference to a drawing and is especially useful with multi-sheet drawings. Although you can zone a drawing in several ways, it is recommended to choose one method and use it throughout all of your designs for the sake of consistency. The method presented in this guidebook includes the following guidelines (see Figure 55):

- The horizontal borders (top and bottom) of the drawing sheet need to be labeled starting with “A” at the top leftmost part of the drawing and increasing alphabetically as you move to the right.

- On the vertical sides (left and right) start with “1” on top and continue downward while increasing numerically as you move down.
- All letters should be capitalized.

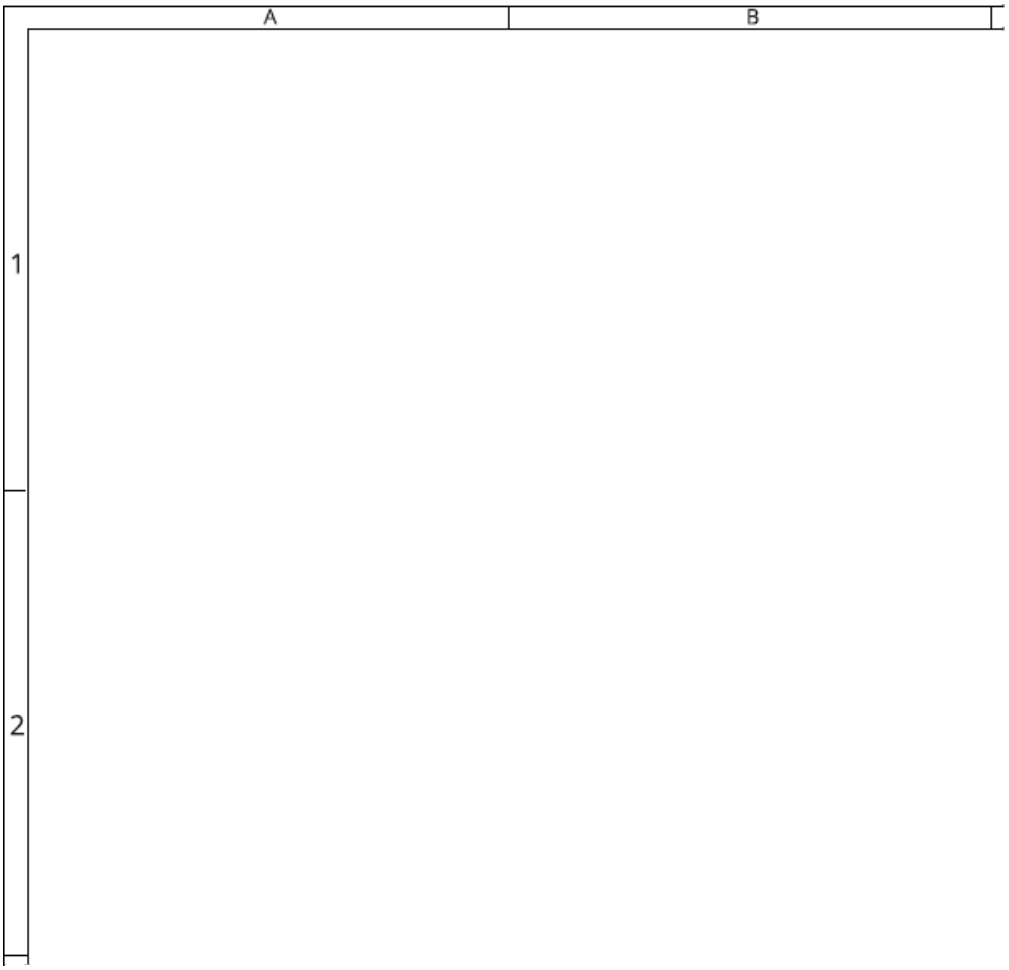


Figure 55 - Example Zoning Method

Title Block

The Title Block is an important part of your PCB design, as it communicates to your manufacturer basic information necessary for manufacturing your board. When creating the Title Block for your PCB project there are many different sections you will need to provide, including:

- Title
- Scale
- Drawing number
- Cage code
- Approval block

The figures below show these sections in detail on the title block and provide additional details about what needs to be included:

Title and Subtitle

The Title and Subtitle provide a brief and accurate description of the PCB and should be written in capital letters

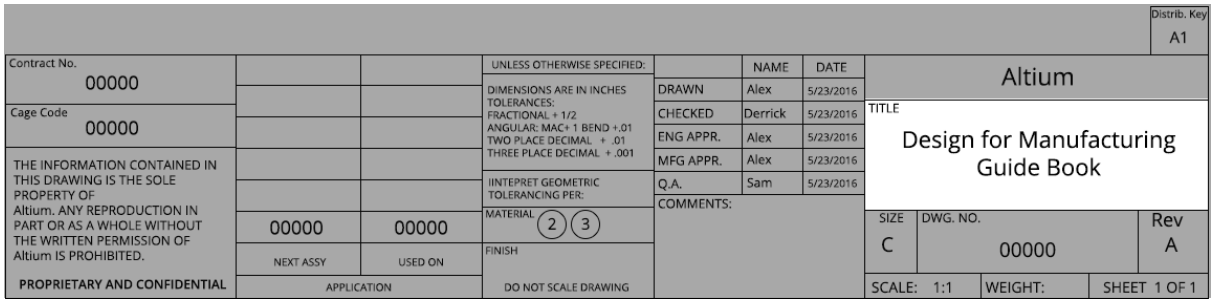


Figure 56 - Title and Subtitle Block

Scale

The Scale is ratio of the actual design to the image and should be described in fractional form.

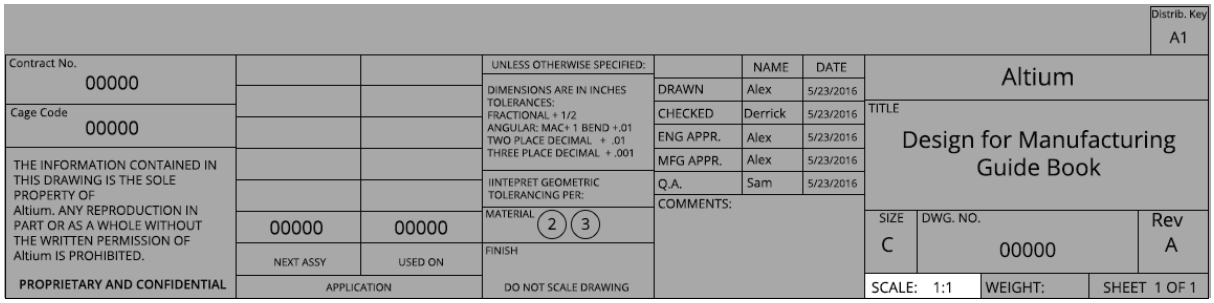


Figure 57 - Scale Block

Drawing Number (DWG. NO.)

The Drawing Number is used for filing and identification of the PCB Project.

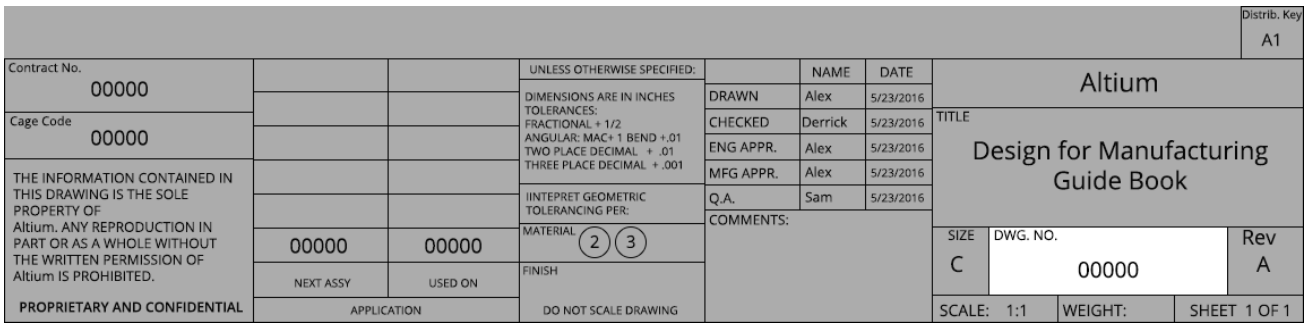


Figure 58 - Drawing Number Block

Cage Code (if applicable)

The Cage Code is a five-character string used by the federal government to identify a business establishment.

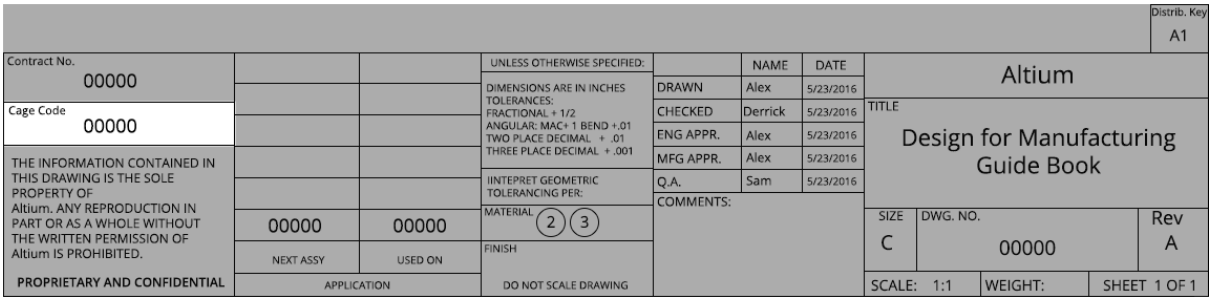


Figure 59 - Cage Code Block

Approval Block

The Approval Block is used to for individuals (drafters, designer, checker, etc.) to sign off on a design.

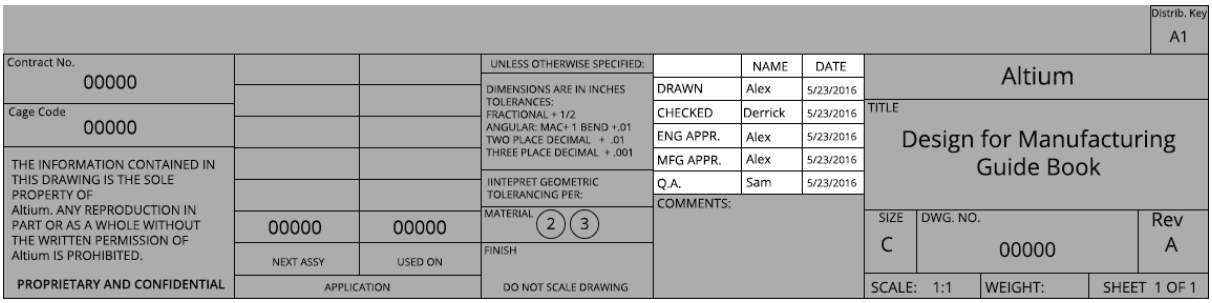


Figure 60 - Approval Block

Although requirements can be different depending on your organization's established CAD standards, the five sections above are considered to be the minimum requirements needed for a title block. You should work to establish your own title block standards for future projects. The blocks shown in the figures below include optional details that might be relevant to your project's specifications.

Application Block

The Application Block is optional and segmented into two parts, the first being the 'USED ON' section and the other being the 'NEXT ASSY' section. The 'NEXT ASSY' section tells the engineer the next assembly the part will be used in, while the 'USED ON' refers to the main assembly that houses the next assembly.

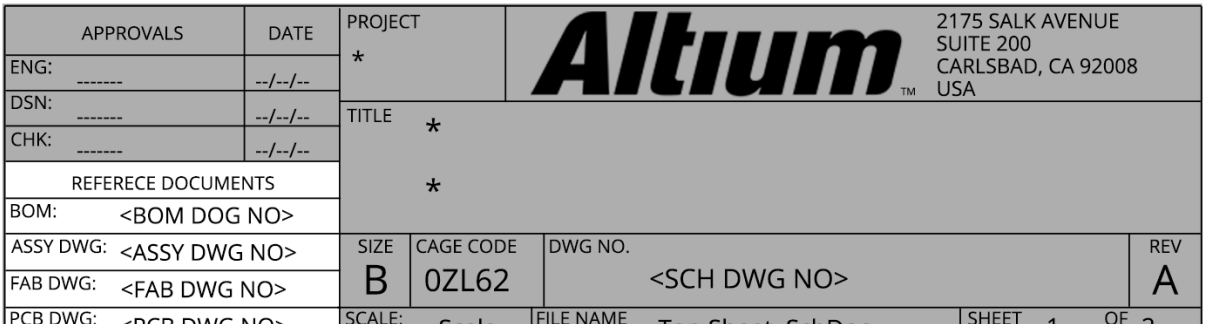


Figure 61 - Application Block

Revision Block

The Revision Block is used to keep track of the project revision and can be seen in Figure 62 below. Make sure to adhere to your company's revision scheme, but if no scheme is in place use the suggested revision scheme below:

- The first revision is shown as an "A"
- The second revision is shown as a "B" and so on
- If you run out of letters introduce a second letter. "AA" → "AB"

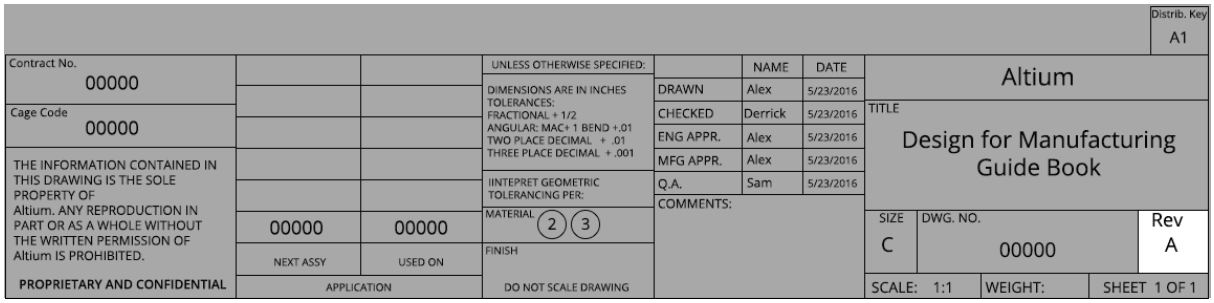


Figure 62 - Revision Block

Contract Number

The Contract Number, also known as the purchase order number, is used to link and track a project.

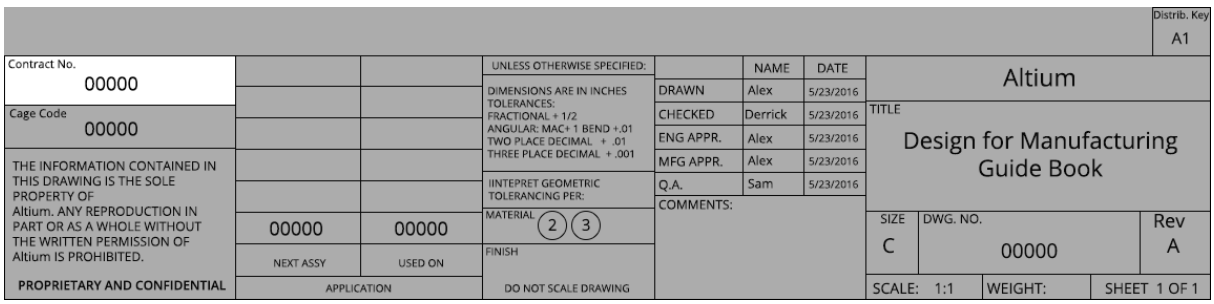


Figure 63 - Contract Number

Distribution Key

The Distribution Key is used for in-house distribution to certain departments in your organization and should be placed directly above the Title Block.

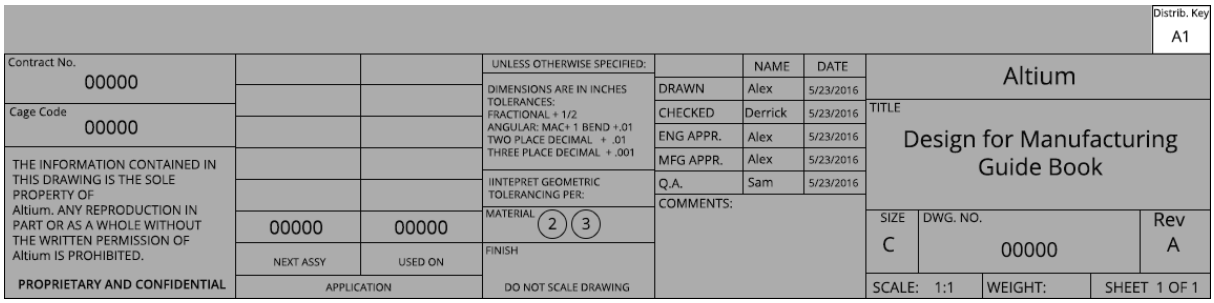


Figure 64 - Distribution Key

Material Block

The Material Block contains numbers corresponding to the appropriate notes, specifying the materials being used.

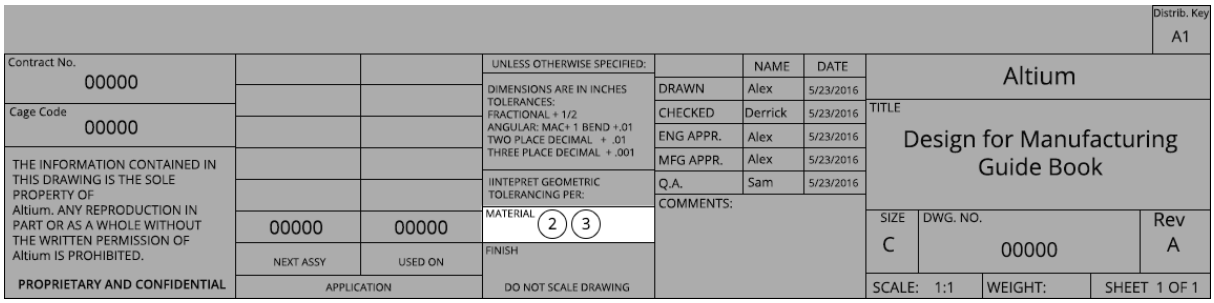


Figure 65 - Material Block

Revision Status Block

The Revision Status Block contains information resides on the first page of the master drawing and shows the revision status for each individual sheet of the drawing. This block should be located at the top-right corner of your PCB template.

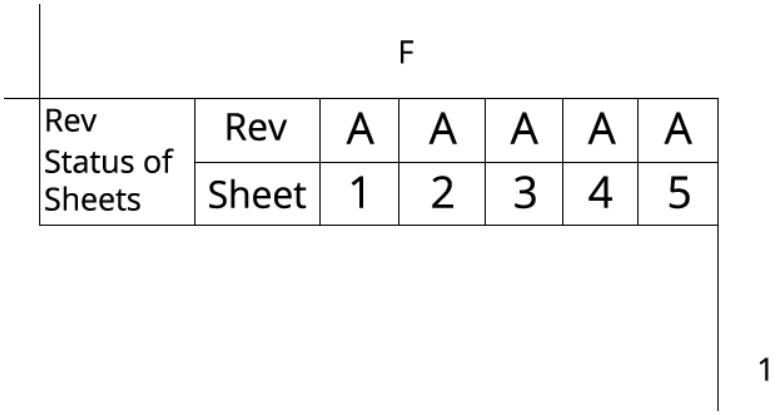


Figure 66 - Revision Status Block

Continuation Sheet Block

The Continuation Sheet Block is used for sheets other than the first page. A Continuation Sheet Block needs to be placed at the bottom right corner of the page as shown in Figure 67 and should include:

- Approval block (if needed)
- Cage code
- Drawing number
- Drawing rev (optional)
- Sheet Number
- Scale
- Size

	NAME	DATE	Rev.	Cage Code 00000	
DRAW	Alex	5/23/2016			
CHECKED	Sam	5/23/2016	A	DWG. NO. 00000	
ENG APPR.	Dan	5/23/2016			
Q.A.	Jeff	5/23/2016	Size C	Scale 1:1	Sheet 6 of 9

Figure 67 - Continuation Sheets

Primary Blocks of a PCB Template for Fabrication and Assembly

Schematic Title Block

While a Schematic Title Block shares much of the same information as its PCB counterpart, including drawing size, date, title and revision (see Figure 67), it also has a number of differences as outlined below:

APPROVALS	DATE	PROJECT	Altium 2175 SLK AVENUE SUITE 200 CARLSBAD, CA 92008 USA	
ENG: -------	--/--/--			
DSN: -------	--/--/--	TITLE * *		
CHK: -------	--/--/--			
REFERENCE DOCUMENTS		SIZE B	CAGE CODE 0ZL62	DWG NO. <SCH DWG NO> REV A
BOM: <BOM DOC NO>				
ASSY DWG: <ASSY DWG NO>				
FAB DWG: <FAB DWG NO>		SCALE: Scale	FILE NAME Top Sheet. SchDoc	SHEET 1 OF 2
<PCB DWG NO>				

Figure 68 - Schematic Title Block

Reference Documents Block

The Reference Documents Block lists the required project production documentation.

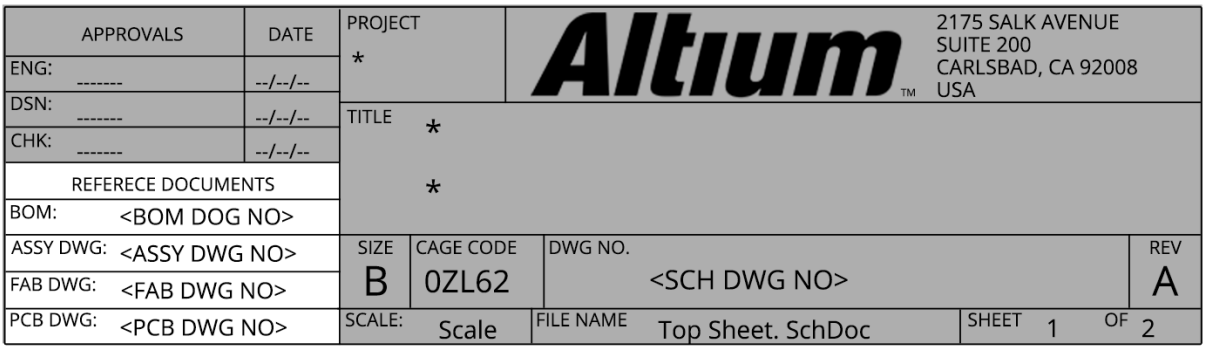


Figure 68 - Reference Documents Block

Assembly Drawing Number

The Assembly Drawing Number is the unique number assigned to the Assembly Drawing. The Assembly Drawing is a detailed depiction of the entire board structure with all components placed.

Fab Drawing Number

The Fab Drawing Number is the unique number assigned to the Fabrication Drawing. The Fabrication Drawing depicts areas on the board that require construction, such as the layer stack and drill table.

BOM Document Number

The BOM Document Number is the unique number assigned to the Bill of Materials (BOM) document. The BOM integrates all aspects of your design to produce your finished product. The BOM is discussed in greater detail later in this guidebook.

PCB Drawing Number

The PCB Drawing Number is the unique number assigned to the PCB Drawing.

Project

This block is used to input the name or number of the main project.

APPROVALS	DATE	PROJECT	Altium	2175 SALK AVENUE SUITE 200 CARLSBAD, CA 92008 USA
ENG: -------	--/--/--	*		
DSN: -------	--/--/--	TITLE *		
CHK: -------	--/--/--	*		
REFERECE DOCUMENTS				
BOM: <BOM DOG NO>				
ASSY DWG: <ASSY DWG NO>		SIZE B	CAGE CODE 0ZL62	DWG NO. <SCH DWG NO> REV A
FAB DWG: <FAB DWG NO>				
PCB DWG: <PCB DWG NO>		SCALE: Scale	FILE NAME Top Sheet. SchDoc	SHEET 1 OF 2

File Name

The file name refers to the saved filename including extension.

APPROVALS	DATE	PROJECT	Altium	2175 SALK AVENUE SUITE 200 CARLSBAD, CA 92008 USA
ENG: -------	--/--/--	*		
DSN: -------	--/--/--	TITLE *		
CHK: -------	--/--/--	*		
REFERECE DOCUMENTS				
BOM: <BOM DOG NO>				
ASSY DWG: <ASSY DWG NO>		SIZE B	CAGE CODE 0ZL62	DWG NO. <SCH DWG NO> REV A
FAB DWG: <FAB DWG NO>				
PCB DWG: <PCB DWG NO>		SCALE: Scale	FILE NAME Top Sheet. SchDoc	SHEET 1 OF 2

Company Name and Address

This area is for your company's name and mailing address.

APPROVALS	DATE	PROJECT	Altium	2175 SALK AVENUE SUITE 200 CARLSBAD, CA 92008 USA
ENG: -------	--/--/--	*		
DSN: -------	--/--/--	TITLE *		
CHK: -------	--/--/--	*		
REFERECE DOCUMENTS				
BOM: <BOM DOG NO>				
ASSY DWG: <ASSY DWG NO>		SIZE B	CAGE CODE 0ZL62	DWG NO. <SCH DWG NO> REV A
FAB DWG: <FAB DWG NO>				
PCB DWG: <PCB DWG NO>		SCALE: Scale	FILE NAME Top Sheet. SchDoc	SHEET 1 OF 2

Finalizing Your Basic Fabrication Documentation

Communicating basic information about your design to both your manufacturer and stakeholders mitigates risks of design intent miscommunication. It is highly recommended to utilize the optional blocks that will best fit your particular project's requirements to facilitate organization of your design documentation. Organized documentation will make it easier for your design intent to connect across your documentation. Now that we have tackled the naming and organization of our documents, let's take a look at the content of the master drawing.

Documenting Your Master Drawing

The master drawing is the most critical part of your design documentation and will convey all of the fine details needed to manufacture your board. While these documentation requirements will change based on the specific design specifications of your PCB, the overall goal is still to clarify your design intent and avoid any manufacturing delays. The master drawing is like the cookbook for your PCB, it includes all the details and instructions on how to manufacture your board. There are specific requirements that you should include in every master drawing, this chapter will show you what those are.

Master Drawing Class Requirements

Documentation requirements for your master drawing will change depending on the class of the board you are designing. The class of the board can be thought as the level of care that you might give the board. For instance, a Class 3 board may be used in medical devices, therefore needing much more thorough documentation than its Class 1 counterpart.

There are three class levels according to IPC-D-325A[7-1]:

Class 1

All that's needed here is the board layout, which acts as the master drawing. Notes will still need to be added to provide the necessary information to your manufacturer.

Class 2

Class 2 requires a master drawing that clearly describes the physical dimensions of the board and includes the following details:

- Pattern features not referenced by hole size or location need to be explicitly dimensioned through notes or referenced by a grid system.
- The coating thickness and plating of the board need to be specified.
- If required, quality conformance test markings can be included in the master drawing.

Class 3

These types of boards require the most documentation and will need to include the details listed in the table below. Manufacturing processes must also be included, such as drilling, plating or etching

Board Details	• Type, size, and shape • Board thickness • Bow and twist, including tolerances • Board layers stack table
Materials	• Type and grade of material; if applicable include color • Marking inks
Hole Details	• Safety markings (UL, ESD, etc...) • Electrostatic discharge • Class 1 - Devices sensitive to voltages of 2,000 or less • Class 2 - Devices sensitive to voltages between 2,001 and 4,000 • Class 3 - Devices sensitive to voltages greater than 4,000 • Marking inks
Processing Conditions	• The location of quality conformance coupons or circuitry • Process specifications and tolerances
Design Concepts	• Include the location of test points • Include the grid system used whether it be metric or inch based • Datums
Documentation	• Include notes and place them on the first sheet or include their location on the first sheet • Artwork Revision • Callouts • Include pattern drawings for each layer of the board

The information in the table above will be presented in detail in the sections to give you a complete understanding of the requirements for each entry.

Board Details

The Board Details defines board complexity and structure.

Board Type

the board type[7-2] specifies the complexity of your board. There are six primary board types that you will want to include on your master drawing:

- Type 1 - Single sided
- Type 2 - Double sided
- Type 3 - Multilayer board through-hole components only

- Type 5 - Multilayer metal-core board through-hole components only
- Type 6 - Multilayer metal-core board with through, blind and/or buried vias

Board Dimensioning

Board dimensioning is a large subject that warrants its own guidebook, this guide will touch on just a few key points as listed below. For a more detailed and complete look at dimensioning please refer to IPC-C-300[7-3] and ASME-Y-14.5[7-2].

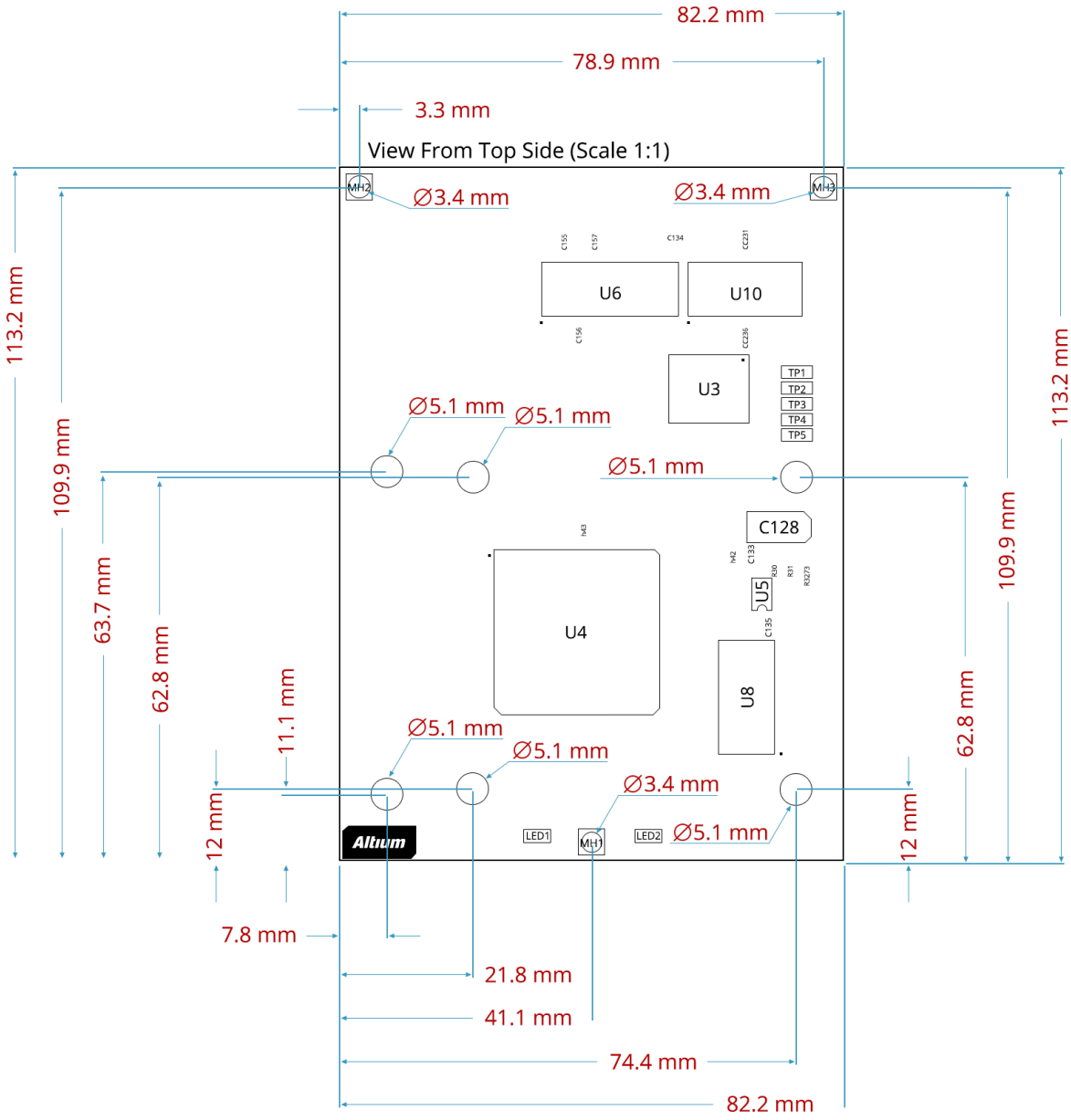


Figure 68 - ADD Well Dimensioned PCB

- You should add a tolerance to each dimension you place.
- Avoid over defining a drawing with unnecessary dimensions.
- Clearly dimension a drawing so that there is only one interpretation.
- Arrange your dimensions to maximize readability.
- Dimension without indicating manufacturing methods, such as what kind of drill bit to use when creating a particular hole.

- Specify the origin to give yourself a reference point.
- Linear dimensions should use a numerical value at its center with arrows in either direction.
- Use a callout when dimensioning holes from a top down view.
- Use linear dimensions when dimensioning holes from a side view.

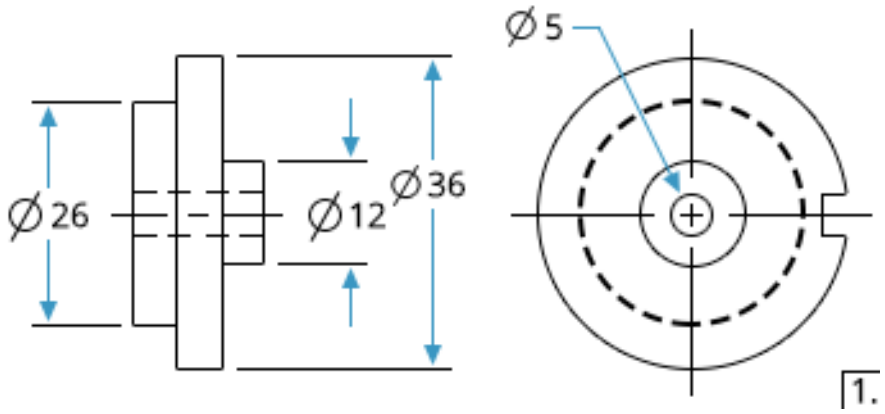


Figure 69 - Dimensioning Holes from a Side View

Callouts

A Callout connects an item with relevant detailed notes.
Callouts are generally utilized to bring attention to a special component or when providing notes with limited space. An example of a callout can be seen in Figure 70 below referencing the notes from the title block.

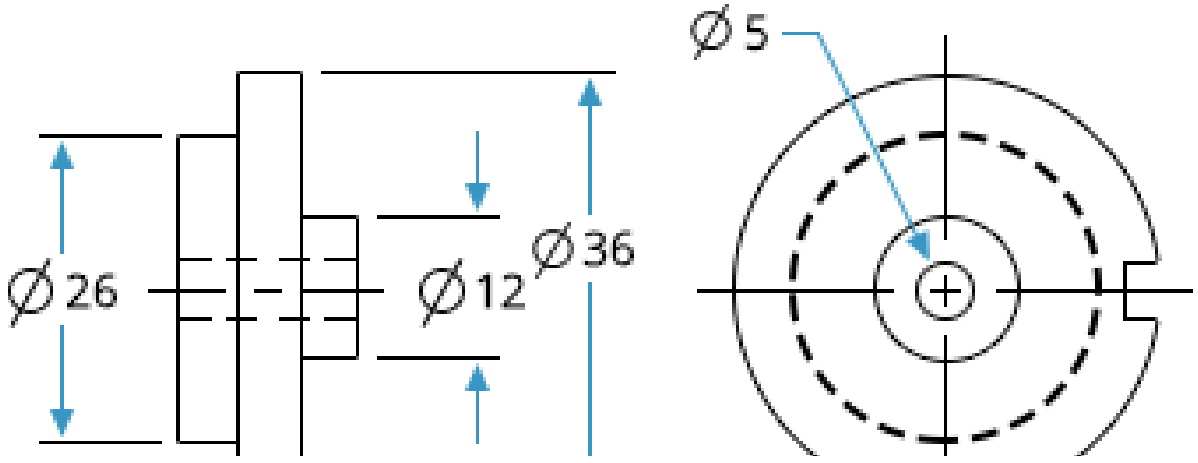


Figure 70 - Callout to notes from title block

Bow and Twist

The Bow and Twist notes tell you how flexible or durable the board is by testing how much a board can bend without breaking.

Bow and twist requirements should be noted on the master drawing.

Board Layer Stack

The Board Layer Stack legend includes details about each layer in your board. It is recommended to include the five columns (Layer, Material, Thickness, Type, and Gerber) as shown in Figure 71 in every project to keep documentation consistent and streamlined across designs.

Figure 71 - Layer Stackup Legend

Materials

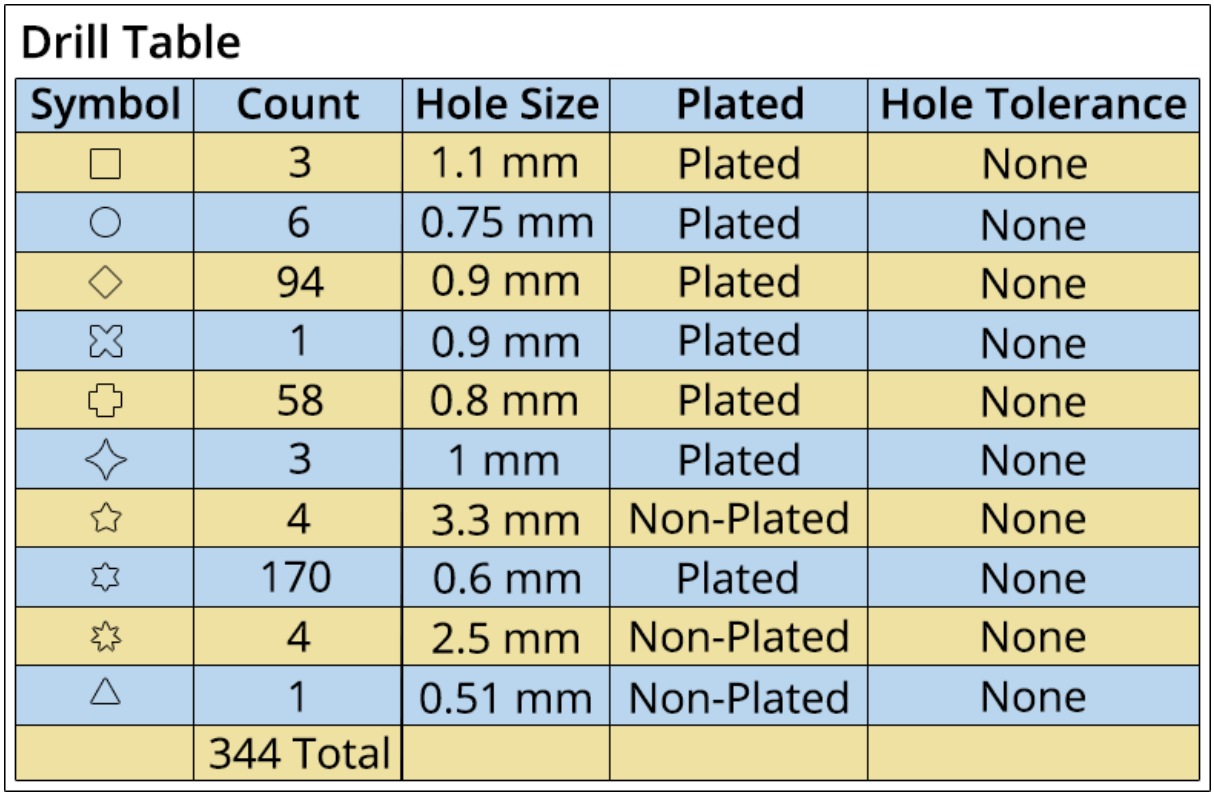
The Materials section defines what materials should be mentioned in the notes section of your master drawing and should specify:

- U.L. requirements
- Laminate type
- Copper foil

The material for the marking inks should also be mentioned. If the marking ink is conductive, then it needs to be properly isolated from the circuitry by spacing it away from other copper or given a coating.

Hole Details

The Hole Details provides information regarding each drill hole. A standard element required to manufacture a PCB is a drill legend, also known as a drill table. The drill table records the specifics of all holes within that board design.
Each drill is represented by a symbol, a letter or the actual hole size. A properly constructed drill table should look like Figure 72 below and includes the symbol, count, hole sizes, hole tolerances, and a column for plating information.



Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
□	3	1.1 mm	Plated	None
○	6	0.75 mm	Plated	None
◇	94	0.9 mm	Plated	None
⊠	1	0.9 mm	Plated	None
⯐	58	0.8 mm	Plated	None
✦	3	1 mm	Plated	None
☆	4	3.3 mm	Non-Plated	None
✡	170	0.6 mm	Plated	None
✡	4	2.5 mm	Non-Plated	None
△	1	0.51 mm	Non-Plated	None
	344 Total			

Figure 72 - Drill Drawing Table

Drill Pattern Drawing

The Drill Pattern Drawing shows all drill locations and can be included as a pen plot, photoplot, or photographic composite copy. This must be produced at a 1:1 scale. The symbols representing the drill bits on the drawing will directly match the corresponding symbol in the drill legend. Figure 73 shows a typical drill pattern documented on a PCB.

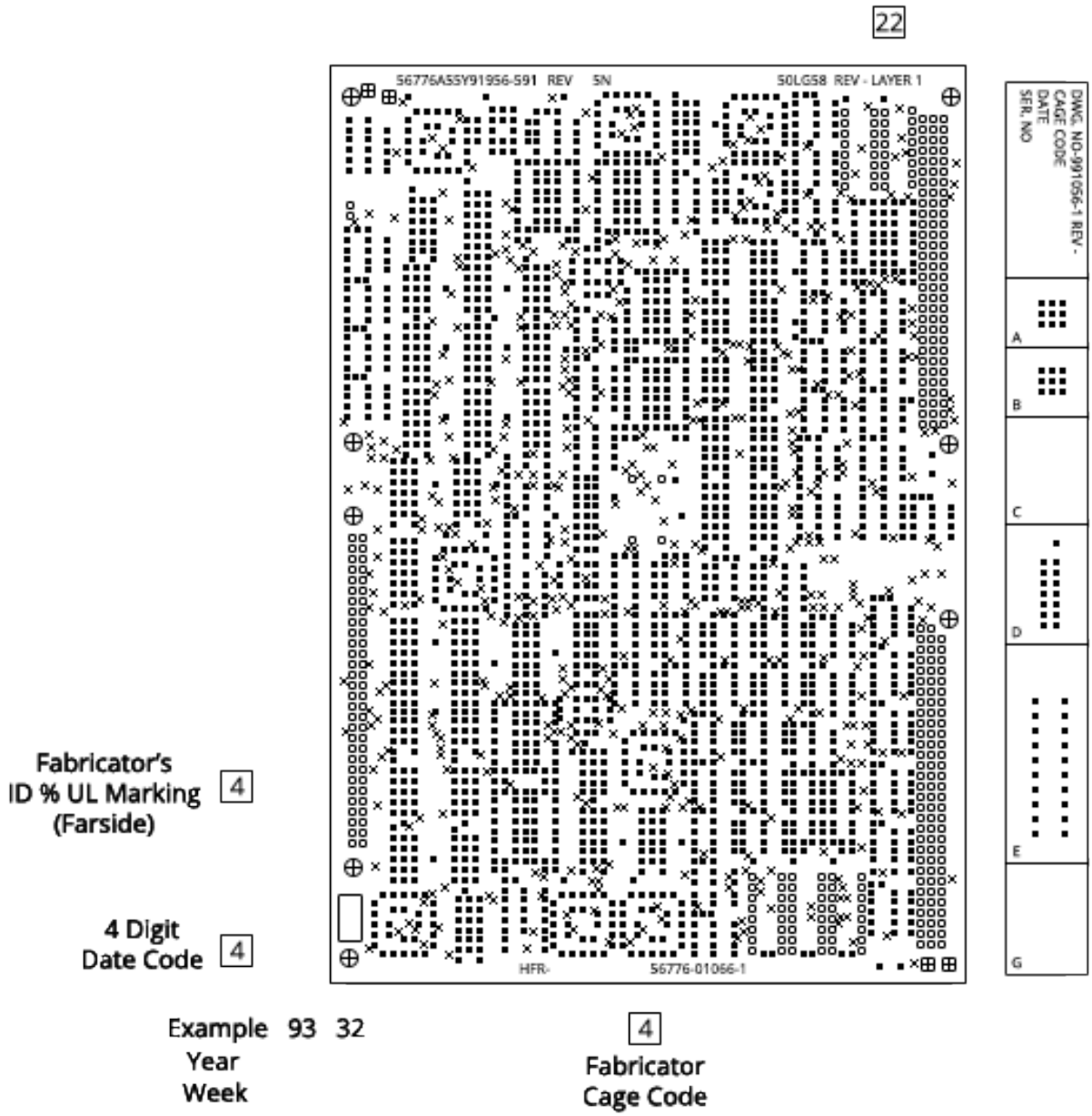


Figure 73 - Drill Pattern on a PCB

Blind and Buried Vias

Blind and Buried Vias, as we have mentioned in Chapter 3, are vias that connect layers, but do not make it all the way to either the top or bottom layer. When working with Type 4 or 6 boards (multilayer boards with blind and buried vias), it is important to specify the location of the vias for each layer pair on the drawing. For the following cases, a separate drill file should be included for each, including:

- Controlled depth holes (from both the bottom and top)
- Blind holes
- Buried holes
- Through-hole drill file

Test Points

Test Points are used to probe areas of your board post manufacturing to ensure quality. You should include test points as part of your drill table and drill pattern drawings. In addition to your fabrication drawings, include your schematic prints with your assembly drawings as it helps with understanding wherein the circuitry your test points are connected.

Markings

Markings are used to show the level of safety associated with your board. The appropriate markings should be placed or noted on the master drawing. In Figure 74 you will notice many countries have their respective markings, and there are even some standards that have a global reach, such as RoHS.

Mark					
Country	Australia	Canada	China	Germany	Finland
Mark					
Country	Italy	Denmark	Norway	Austria	Poland
Mark					
Country	Sweden	Switzerald	America	Europe	Germany
Mark					
Country	Germany	England	America	America	America
Mark					
Country	Japan	Japan	America	America	Saudi Arabia
Mark					
Country	Holland	The Globe	Germany		

Figure 74 - Safety Level Markings

Restriction of Hazardous Substances (RoHS)

The Restriction of Hazardous Substances (RoHS) standard is used throughout the world[7-4]. The RoHS standard restricts the use of substances, such as lead and mercury in electrical and electronic equipment as they are hazardous to the environment and humans. Markings for RoHS should be placed or noted on the master drawing. Figure 75 shows some RoHS compliant markings.

Figure 75 - RoHS Marking Labels

Underwriters Laboratories INC. (UL)

One marking not mentioned above is the “UL” marking. Having UL recognition for your board means that your base materials and design were manufactured through UL-approved processes. The board also meets their standard for thermal shock, plating adhesion and bond strength. For more information on this standard, refer to the UL 796[7-5] standard for printed wiring boards. The UL marking should be indicated on the drawing or notes like all other markings.

Electrostatic Discharge (ESD)

The markings in Figure 76 are electrostatic discharge markings and are placed on a static sensitive board[7-1]. If there is enough space, markings may be added to the board via silkscreen. Make sure that these markings are visible on both the board (if applicable) and master drawing.

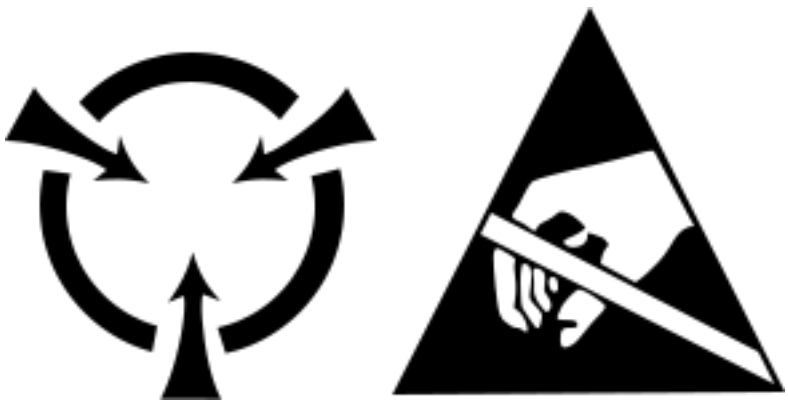


Figure 76 - Electrostatic Discharge Markings

Marking Inks

Marking Inks are used to create drawing labels and markings. When placing markings on a board one should avoid putting markings on conductive surfaces, surfaces that will be covered with melting metals, and places that are hidden from view. The master drawing should be marked with some fixed format information including part number, layer number, revision level, and orientation symbols.

When applying ink, labels, laser scribes, or any other markings you should take care to ensure they are non-nutrient, non-conductive, high contrast, and durable enough to survive manufacturing.

Processing Conditions

The Processing Conditions include details about how your board will be produced during manufacturing and assist your manufacturer to efficiently optimize their equipment for your particular design requirements.

Quality Conformance Coupons

Quality Conformance Coupons, also known as test coupons, are small PCB sections used for testing and are made at the same time as the primary board. They are used for testing a variety of variables includes impedances and inter-plane capacitance. These quality conformance circuitries should appear on the master drawing as they appear in the PCB panel.

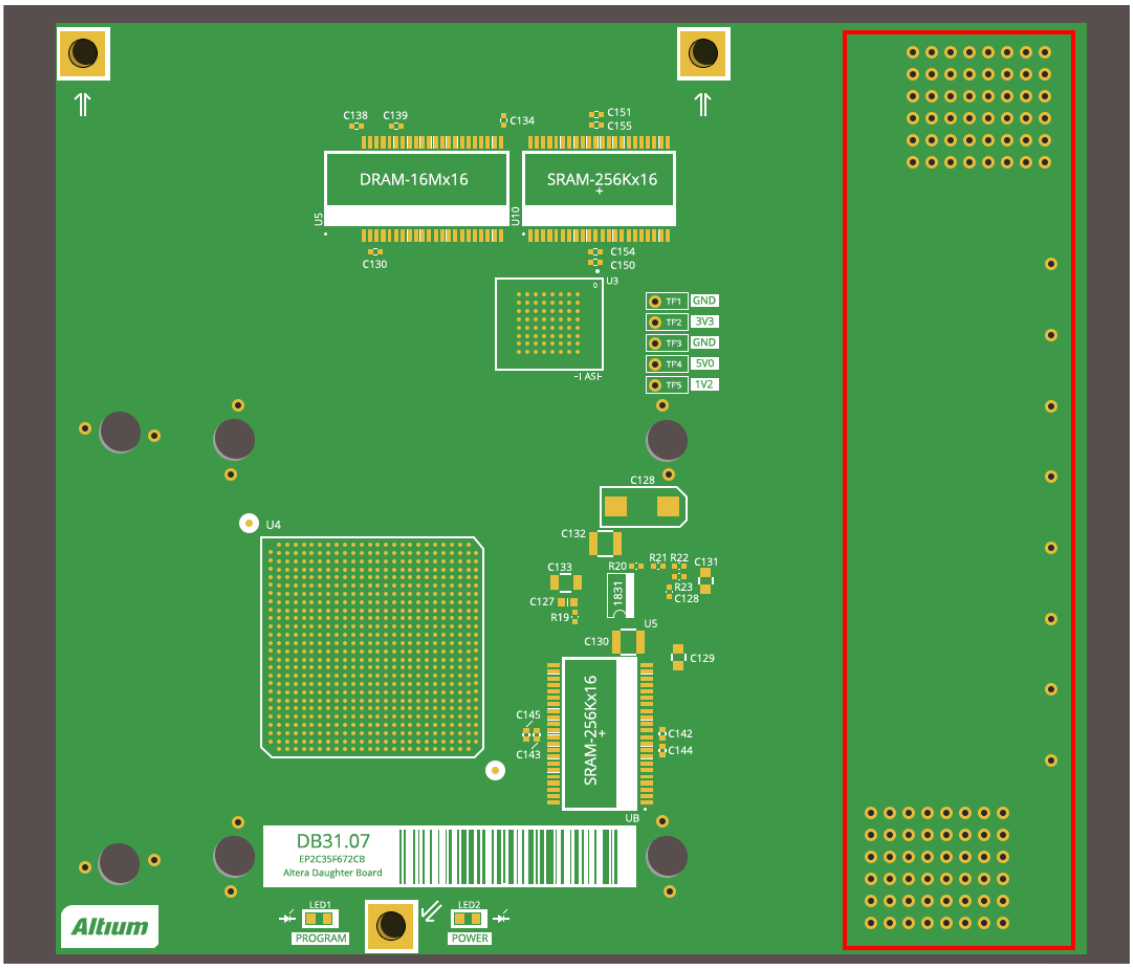


Figure 76 - Quality Conformance Coupons

Process Specifications

Process Specifications include the information a manufacturer needs when performing certain processes, such as cleaning and preparing your board. The process information should include information regarding tolerances. For example, when creating a solder mask, you want to have its thickness set at .002” with a tolerance of .001”.

Grid System

The Grid System plays an important part in the creation of boards and is used for the location of features and items including components, plated through-holes, and surface mount land patterns. Features not residing on the grid, need to be dimensioned with a given tolerance. Make sure that your grid systems are always within a minimum of two datum points and that you specify the grid increments on the master drawing.

Manufacturing Features

The Manufacturing Features include additional information that will allow your manufacturer’s machinery to see how a board is oriented in space for efficient processing.

The proper alignment of your board is vital to avoid registration issues and is achieved through datums.

Datum

A Datum is a reference point located on the printed board, usually a hole, that allows a machine to “see” how the board is oriented in space. For more detailed information, please refer to IPC-D-300[7-6].

You should choose datums as functional features located on the grid that relate to connecting parts such as screws or mounting holes. Avoid choosing datums at a board’s edge as they may not adequately characterize the board’s function.

To establish the grid with respect to the board, at least two holes need to be placed on the grid. These holes need to be properly dimensioned with respect to a datum references and will also create an origin for the board.

Fiducial Targets

Fiducials are a specific type of datum usually used for pick and place machines and allow the machine to know where the PCB is oriented in space. Fiducial targets must be shown on all surface mount artwork.

Master Drawing Documentation

The Master Drawing Documentation section of your master drawing includes all supporting details for your PCB including notes, callouts, and additional artwork to help clarify your manufacturing intent.

Artwork Configuration Control Chart

The Artwork Configuration Control Chart is a drawing that identifies and manages the revision levels of various artworks including silk screens, solder paste, and NC drill data.

Artwork	DWG. No.	REV level	Cu WT. OZ.	Nom. finished line width
Gerber plot data:				
Primary side: (horiz) signal Layer"1"	991793	A	1/2	.007"
Inner signal layer (vert) signal Layer"2"	991793	A	1	.007"
Ground player Layer"3"	991793	A	1	-
VCC plane (+5 volts) Layer"4"	991793	A	1	-
Inner signal layer (horiz) signal Layer"5"	991793	A	1	.007"
Secondary side (vert) signal Layer"6"	991793	A	1/2	.007"
Solder mask (top)	991793	A		
Solder mask (bottom)	991793	A		
Solder mask (top)	991793	A		
Solder paste screen (top)	991793	A		
N.C, Drill data - PC board	991793	A		
Bare board test data IPC-D-356 format	991793	A		

Figure 4-6 Artwork Configuration Control Chart, 6 Layer Board

Figure 77 - Artwork Configuration Control Chart

The Rev Level column summarizes the revision of the individual artwork, and the Cu. WT. oz. column shows the copper weight of the individual layer. Include this chart on the first page of your master drawing.

Notes

Notes accompany the fabrication drawings and are used to communicate your requirements and details for the fabrication process. Below is a list of possible notes that you might want to include with your drawings:

- Finished board specifications and class
- Material requirements
- B-stage material requirements (for multilayer boards)
- Board markings
- Construction
- Solder mask specifications
- Solder mask material & thickness
- Drilled hole requirements
- Copper plating thickness
- Etchback requirements
- Bow and twist requirements
- Silkscreen ink type
- Test coupon requirements
- Bare board electrical test requirements

Example Notes from IPC-D-325A[7-1]

- Fabricate boards in accordance with IPC-RB-276[7-7], Class 3. Finished boards must meet quality conformance testing and inspection as specified.
- Material in accordance with MIL-S-13949/4[7-8], laminated sheet, HTE copper-clad, type GF glass cloth base, flame resistant (meeting UL 94V-1 or better). Tg rating: 140 to 160 C
- Material in accordance with MIL-S-13949/12[7-9], plastic sheet, type GF base material, glass base pre impregnated (B-stage), Tg rating: 140 to 160 C.
- Board fabricator shall apply date code, fabricator's cage code, I.D. and UL marking to primary side and secondary side where indicated. Marking to be copper etched.
- Construction to be solder mask over bare copper (SMOBC), using Type XXXX, photoimageable dry film, 0.003 in thick. Apply to primary and secondary sides in accordance with IPC-SM-840[7-10], (type B, Class 3). Use appropriate solder mask artwork for each side of board. Puncturing of tented holes is not permissible.
- Solder mask misregistration shall not exceed +0.004 in. Solder mask overlap permitted on circular lands only, and shall not exceed 0.001 in. No overlap permitted on SMD rectangular lands
- Solder mask thickness: 0.002 in min./0.003 in max. Solder mask material to be light green in color and highly transparent
- Drill boards using drill data, drill pattern and hole schedule. Hole locations may vary within .004 in (Radial Error) max. about true position.
- All holes are plated-through unless noted otherwise.
  Minimum copper plating in plated holes to be .001 in.
  Copper plating in tented holes shall not plug holes closed.
- Dimensions are after etching and plating, and are basic unless otherwise indicated.
- Bow and twist shall not exceed 0.0075 inch per inch measured in accordance with IPC-TM-650[7-11], method 2.4.22.
- Silkscreen primary side (top) and secondary side (bottom) of board using white epoxy base ink per MIL-I-43553[7-12], Type II, and appropriate artwork.
- Test coupon: place fabricator's cage code, date code or serial no. where indicated, using white epoxy ink or copper etch. One metallographic specimen shall be tested and supplied with each lot of boards. A report of measurements, showing average plating thickness and quality, shall be supplied with each specimen. Testing shall include thermal stress and microsectioning per IPC-TM-650[7-13], Methods 2.1.1 and 2.6.8[7-14]. Each specimen shall be identified and traceable back to the originating lot.
- Bare Board Electrical Test: Bare boards shall be electrically tested using CAD generated net list data. This information to be supplied in IPC-D-356[7-14] format.

Electrical testing shall follow the guidelines established by IPC-ET-652[7-15], guidelines and requirements for electrical testing of unpopulated printed boards.

Completing Your Fabrication Documentation

Your design documentation is arguably one of the most important components of your design process. Even the greatest PCB design will go to waste, if you are not able to clearly communicate design intent to your manufacturer. With your master drawing completed, you now have everything you need to get a bare board produced by your chosen fabricator. In the next chapter we will explore the last piece of the documentation puzzle for the final assembly of your PCB.

Documenting Your PCB for Assembly

With your fabrication (bare board) requirements documented, it is now time to move on to an equally important stage - documenting the instructions for component placement and final assembly. It is in the assembly stage where your bare board is brought to life with all the components you specify in your Bill of Materials. This chapter will cover what you need to know to have your board successfully assembled and will cover assembly drawing requirements, adding notes, and placing cautionary markings.

Assembly Drawing Requirements

The Assembly Drawing Requirements define the final board assembly and provide specific instructions to your manufacturer on component placement, orientation, and identification. You will want to include the following details as part of your assembly drawing documentation:

Location of components	Reference dimensions for envelopes	Conformal coating requirements
Reference designations for all parts	Component mounting and spacing installation requirements	Mechanical hardware including latches and mounting hardware
Orientation and polarity of components	Special solder plug or masking requirements	Cleanliness requirements
Required structural details for support and rigidity	Electrostatic discharge label	Workmanship specifications
Requirements for markings and lead forming	Electrical test requirements	
Specific soldering requirements including solder paste	Eyelets and terminals	

Required Assembly Documentation

The Required Assembly Documentation consists of a number of assembly drawing templates that you will need to include with your final design including schematic prints and a finalized BOM. In addition to your notes, these drawing templates will allow your manufacturer to clearly understand your design intent for final component placement and assembly.

Schematic Prints

The Schematic Prints outline your intended board component connections and are necessary to define and establish your required test points.

During the final testing process, your board tester may be able to find your test points on the physical PCB, but for greater clarity they'll utilize your schematic prints to understand how those test points connect to your network of circuitry. Figure 78 shows a sample schematic with defined test points.

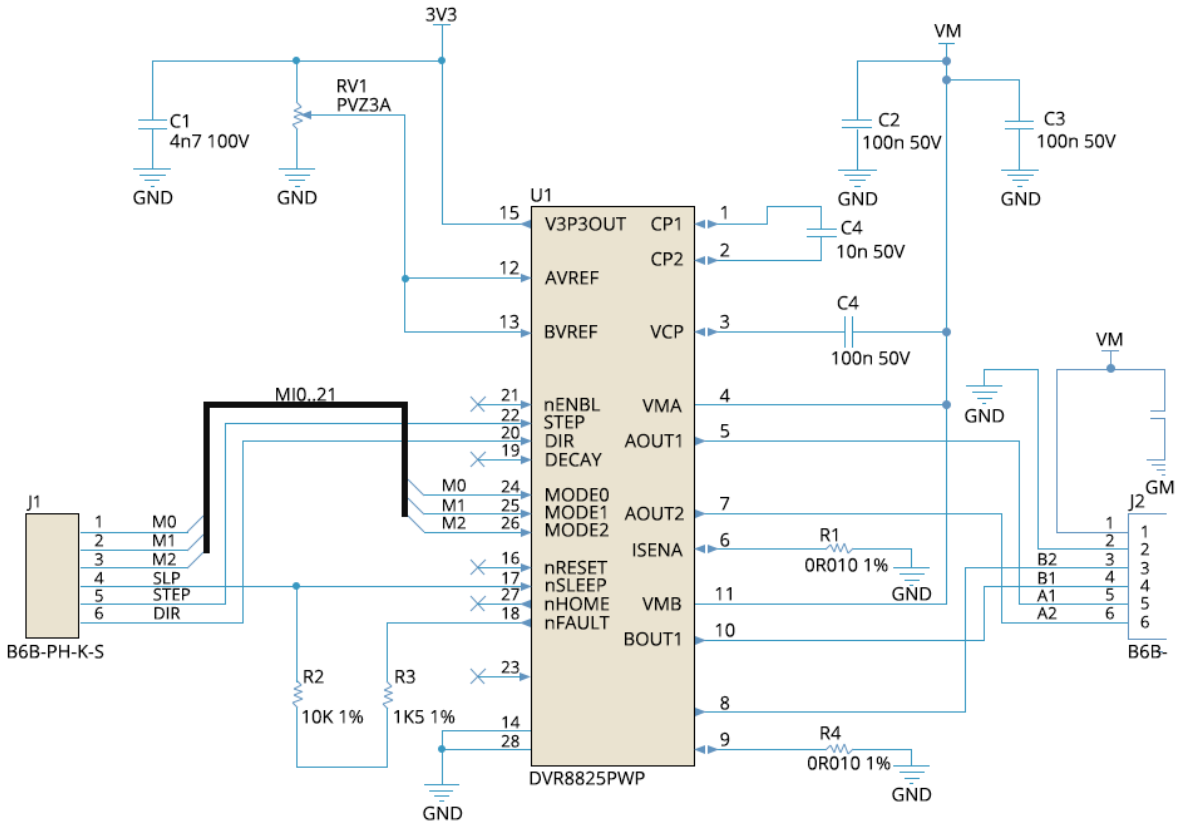


Figure 78 - Schematic Prints

Bill of Materials

The Bill of Materials will include a detailed and sourceable part list that includes all necessary part supplier information. Providing a BOM to your manufacturer with included component designators and supplier information ensuring your design will be manufactured with the appropriate parts. The BOM is covered in depth later in the guide. Figure 79 below shows a sample BOM with some of the necessary part information you will want to include:

Bill Of Materials

Item #	Footprint	Designator	Quantity
1	C0603	C1	1
2	C0603	C4	1
3	C0603	C2, C3, C5	3
4	C1206	C6	1
5	B6B-PH-K-S	J1, J2	2
6	R1206	R1, R2	2
7	R0603	R3	1
8	R0603	R4	1
9	PVZ3A	RV1	1
10	PWP28_5P18X3P1	U1	1

Figure 79 - Bill of Materials

Cautionary Markings

Cautionary Markings are very important for safe handling of your board. As part of your assembly documentation, you will need to include the electrostatic discharge markings shown in Figure 80 if your board requires special handling due to static sensitivity.

Figure 80 - Electrostatic Discharge Markings

In addition to the symbols above, the notes in the table below need to be placed above or as close to the title bar as possible. The notes used depends on the class of your board, and markings can be applied using copper etching or silk screening[8-1].

Class 1 & 2 Boards	"ELECTROSTATIC DISCHARGE CONTROL PROGRAM FOR PROTECTION OF ELECTRICAL AND ELECTRONIC PARTS, ASSEMBLIES AND EQUIPMENT SHALL BE IN ACCORDANCE WITH MIL-STD-1686, CLASS _____ AND MIL-HDBK-263."
Class 3 Boards	"ELECTROSTATIC DISCHARGE CONTROL PROGRAM FOR PROTECTION OF ELECTRICAL AND ELECTRONIC PARTS, ASSEMBLIES AND EQUIPMENT SHALL BE IN ACCORDANCE WITH MIL-STD-1686, CLASS 3, AND MIL-HDBK-263

Refer to the guidelines below if you are unsure about which class your board is:

- Class 1 - Devices sensitive to voltages of 2,000 or less
- Class 2 - Devices sensitive to voltages between 2,001 and 4,000
- Class 3 - Devices sensitive to voltages greater than 4,000

Notes

Assembly drawings, like fabrication drawings, require their own set of notes. These notes include information about the merging of the board with its components, including assembly standards, handling instructions and solder specifications. There's no such thing as too much detail in your assembly documentation. If you think your manufacturer needs to know something about a specific component's placement or assembly requirements, make a note for it. Below are some examples of assembly notes as seen in IPC-A-325A[8-1]:

- Workmanship to be equal to and compliant with the requirements of IPC-A-610.
- Mark group (or dash) number, revision and serial number as shown; marking to be 0.10"-high characters using item no. 6, white epoxy ink, per MILI-43553, type II.
- This assembly contains electrostatic discharge (ESD) sensitive devices; static-free handling is required per MIL-STD-1686, class 2
- Conformal coating is not required.
- Designations are for reference only and do not appear on individual parts.
- Dimensions shown specify maximum envelope limits for the finished assembly.
- Orientation of polarized capacitors is denoted by a plus (+) sign. Polarity is identified on the part.
- Dot identifies pin #1 location and device orientation when viewed from the top.
- Using solder paste screen, apply solder paste, item #4, to primary side of board.

Completing Your Design Documentation

This chapter concludes the last and final link needed to successfully document your PCB for both fabrication and assembly. With a completed board layout in hand and all of the details documented to successfully communicate your manufacturing intent, you're now ready to ship your design files off to manufacturing to begin the production of your board. The final chapter in this guidebook will dive into the specifics of each file you will want to send your manufacturer as part of your completed board layout and documentation.

Preparing Your Manufacturing Files

With your PCB fully designed and documented, it is now time to turn your focus towards delivering all of those design assets to your manufacturer. This is where manufacturing files come into play, and it is this group of output files that will be responsible for clearly communicating your design intent to begin the fabrication and assembly process.

Every file that you deliver to your manufacturer includes a critical piece of design information necessary to align both the machinery, manpower, and specifications needed to successfully produce your board in a manufacturing facility. This chapter will summarize the details you need to know about each manufacturing file including Gerbers[9-1], ODB++[9-2], and IPC-2581[9-3]. By the end of this chapter, you will know exactly what files need to be sent to your manufacturer to put the finishing touches on your design process.

Basics of Manufacturing Files

It is important to know exactly what outputs your manufacturer requires and understand what information is included in each of these files. By ensuring that you include all of the necessary files as part of your output documentation, you will minimize the potential for errors in the manufacturing process and eliminate any dependencies on respins. It is recommended to use industry standards to describe the process you want your manufacturer to use. IPC specifications often provide a more detailed method for fabrication than standard descriptions can provide as they have been highly refined to remove any ambiguity from their specifications.

Once you've finished your design process in your software, you will begin the process of outputting each manufacturing file. These output files are listed in five categories in the table below, with each having a number of different specifications you will need to know about.

Assembly Outputs	Documentation Outputs	Fabrication Outputs
• Assembly Drawings • **Pick and Place files**	• Composite Drawing • 3D Prints • PCB Prints • Schematic Prints • Simulation Prints	• Composite Drill Guides • Drill Drawings • Final Artwork Prints • **Gerber Files** • Solder/Paste Mask Prints • **NC Drill Files** • **ODB++ Files** • Power-Plane Prints • **IPC-2581**

Netlist Outputs • **IPC-D-356**		Report Outputs • **Bill of Materials** • Component Cross Reference • Project Hierarchy • **Test Point Report**

Now, we will demonstrate some of the primary manufacturing files[9-4] that you will need to be concerned with and provide outline the necessary details needed to successfully generate your output documentation.

Gerber Files

Gerber files are the industry-standard file format for PCB manufacturing and were developed by Gerber Systems Corp, now Ucamco, over 35 years ago. The Gerber format can be split into two major categories:

- Standard Gerber, or RS-274-D, which was later replaced by RS-274X.
- Extended Gerber, or RS-274X, widely used today.

The development of the Standard Gerber format kicked off the era of PCB manufacturing with vector photo plotters but quickly lost relevance as technology advanced and raster plotters gained popularity. Extended Gerber was later introduced in the late 90's to eliminate the limitations of Standard Gerber.

The solidification of Extended Gerber as the leading file format for PCB manufacturing reached its peak when Ucamco declared Standard Gerber obsolete in 2014[9-5]. Since then, Extended Gerber has been further revised to create Gerber version 2, commonly referred to as X2. Gerber X2 introduces new attributes that allows the file format to provide metadata on included images and components.

Standard Gerber (RS-274-D)

Standard Gerber, or RS-274-D, is essentially obsolete and should no longer be used for manufacturing. Modern day Gerber files should instead be produced in the RS-274X or Extended Gerber version 2 file format, as these files provide more detailed and cleaner information about your design intent for manufacturing purposes.

Extended Gerber (RS-274-X)

An Extended Gerber[9-6] file provides a series of single, resolution-independent images of graphic objects. By assembling these objects together, this file type provides a unified image of each layer of your board layout including defined sizes, shapes, and locations of real-world components.

This file is composed of a collection of commands that control both the graphic states and graphic objects used to produce the image of your PCB layers.

Each file in RS-274-X corresponds to a single layer and contains all of the information needed to recreate that layer in its physical form. The logical commands found within each Gerber are structured and executed in a linear fashion, and these commands manipulate the graphic objects and alter how they are generated. These commands can be split into two types:

- Function code commands are single letter codes beginning with D/G/M and a positive integer.
- Extended code commands are two letter codes paired with the ‘%” sign.

These commands then manipulate various graphic objects found in every Extended Gerber including:

- Draw objects which produce a straight line with thickness and endings dependent on the shape of the current aperture.
- Arc objects which utilizes the current aperture to create circular segments and always has rounded endings.
- Flashes which are reproductions of apertures that are often reproduced many times and are commonly used to create pads.
- Regions which are sections defined by linear and circular segments and are commonly used for copper pours.

Both the commands and graphic objects above interact with apertures in an Extended Gerber file, which are simple 2D geometric symbols with an origin point used to center along listed coordinates. There are two kinds of aperture templates, including:

- Standard Apertures include circle (C), rectangle (R), obround (O) and regular polygon (P).
- Macro apertures are identified by their given name and defined shape formed by linking and parameterizing primitives.
-

When an aperture is used, it is set to the ‘current aperture’ and added to a template dictionary. Every standard aperture is used to create a set of primitives that can be utilized to create macro apertures.
The concepts above all tie together to create a completed image of your board layers using polarity. There are two types of polarity found in an Extended Gerber including:

- Clear Polarity, which clears its shape through all levels of a plane.
- Dark Polarity, which darkens its shape on the top level of a plane.

A completed image of a board layer results from a composite of overlaying graphic objects combined with both of these polarities.

Extended Gerber Version 2 (X2)

Extended Gerber Version 2, or X2, operates using the same principles and concepts of an Extended Gerber and is fully backward compatible with Extended Gerber machinery. New attributes were introduced in the X2 version, which includes added metadata for graphic jobs. This metadata provides additional information and details about component features and use cases and helps your manufacturer to seamlessly transition from design files to a physical fabrication process and ultimately reduces fabrication time and errors.

Generating Gerber Files

Understanding the structure of Gerber files is key to their proper setup[9-7]. Start by determining the units you want to use, being either inches or millimeters. Then, select the specified format of your coordinate data which allows you determine the precise placement of objects in your PCB workspace. There are several resolution formats to choose from, including:

- **2:3** which has a resolution of 1 mil (1/1000 inch)
- **2:4** which has a resolution of 0.1 mil
- **2:5** which has a resolution of 0.01 mil
- **2:6** which has a resolution of 0.001 mil

The 2:4/2:5 format will be required if you are using a grid less than 1 mil, or objects have a resolution of less than 1 mil. Contact your Manufacturer for exact format and resolutions.

Each layer selected will plot into an individual Gerber file with its own unique extension. It is important to confirm that every layer is exported into its respective Gerber file as missing or incorrectly placed layers can often delay your fabrication process.

Most modern photo plotters in use today are raster plotters which can accept any size aperture, including Gerber files with embedded apertures.

Virtual Film and Final Setup

The last part of your Gerber file setup process involves setting the size of the virtual film and its border size, as well as matching aperture tolerances and configuring zero suppression settings. Your Gerber files should be created with the same format and precision as your NC drill files.

> *Example: The Gerber files have been configured to use the 2:5 format, then the matching drill files should use the same format. The same would be for absolute or relative origin.*

Manually Generating Your Gerber Files

There are some guidelines to follow when manually generating Gerber files, including:

- All files should use current constructs and avoid S-274-D as it is now a deprecated file format.
- Use a resolution for your units that provides a clear image of your design.
- When using imperial and metric units, provide 6 and 5 decimal places respectively.

With your Gerber files setup and generated, it is time to move on to generating your ODB++ files for your manufacturer's CAM system.

ODB++ Files

The original ODB file format was developed in 1995 by Valor as an alternative to Gerber files. ODB++ was later released in 1997 with the addition of component names to the original ODB format. Valor's goal was to expedite the communication of design intent from design to manufacturing by simplifying data exchange between CAD and CAM systems. ODB++ achieves this goal by consolidating information about your PCB design into a zipped file that can then be loaded into CAM systems.

The CAM tools in use today can easily analyze ODB++ files to extract all information about your design including size, shape, position, and features of all your design elements including components, pads, vias, etc. These design elements are defined within an ODB++ file and allow for easy recognition by manufacturing CAM tools.

Some companies prefered using the IPC-2511 standard (GenCAM) instead of ODB++, however, ODB++(X) was recommended by National Electronics Manufacturing Initiative (NEMI) in 2002[9-8] to help merge the standards to a more open format, and this recommendation gained traction with support from several prominent companies including Nokia, Hewlett-Packard, and Xerox.

Understanding the ODB++ File Structure

ODB++ files resemble the file structure of operating systems and can be preserved in a single, compressed file. The structure[9-9] of ODB++ files provides incredible diversity for conveying information about your PCB design, from BOMs and layer stack ups to test point netlists and fabrication data. A complete, zipped ODB++ file comprises all information needed for manufacturing and assembling your board design, and the files are loaded into a front-end CAM system to direct the manufacturing process.

Although commonly referred to as ODB++ files, ODB++ can be more accurately be described as a file structure. An ODB++ description of your design will only exist as a single file for the purpose of conveying design intent to your manufacturer. Typically, an ODB++ file structure will be converted into a "tarball" and then zipped. Figure 81 shows an example hierarchy of an ODB++ file:

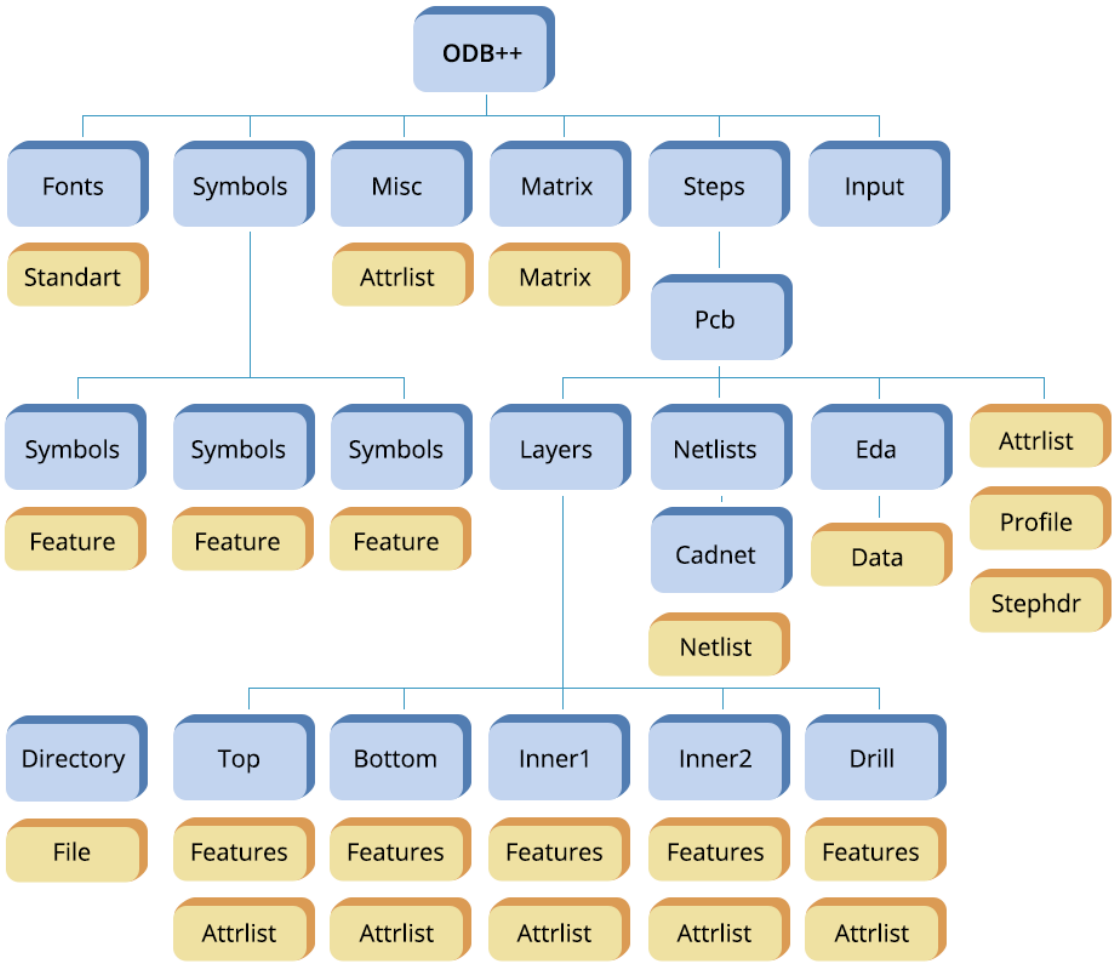


Figure 81 - ODB++ File Structure

Why You Should Use ODB++

Designs documented by Gerber require conversions to successfully process, and this time-consuming process adds additional time needed to manufacture your board.

Using ODB++ files help to resolve this issue with:

- An organized file structure that allows for a detailed design description providing designers and manufacturers with clear board specifications.
- A single source of truth for manufacturing files in one compressed package that doesn't need to be converted or translated by your manufacturer.
- An organized file structure that provides a singular data structure for utilization between fabrication, assembly, and testing.

Generating ODB++ Files

Begin by enabling the specific layers that you want to plot as part of your generated output files[9-10]. In a similar fashion to Gerber file generation, you can also select which mechanical layers to add to all ODB++ layer plots. You will need to specify the source that is to be used to create the ODB++ Profile layer. This Profile layer contains the enclosing boundary of the board usually set by default to the board outline.

The board outline, also referred to as the board shape, is a closed polygonal shape that defines the boundary of your PCB and is one of the best sources for creating a Profile layer. If your design has no associated board shape, you can choose a different PCB layer to define the closed polygon representing the boundary of the board (e.g. the KeepOut layer or a specific Mechanical layer).

A job in ODB++ is represented by a self-contained directory tree which can be transferred between computer systems or even version controlled without loss of data. A database job is a single folder (odb), composed of the following sub-folders:

- Fonts
- Input
- Matrix
- Misc
- Steps
- Symbols
- User

The steps folder contains various sub-folders including the folder layers, which contains output for each layer enabled for plotting in the ODB++ setup dialog, as well as drill information and component information. The symbols folder contains single layer graphic objects which can be recalled in any graphical layer in a specific step. The matrix folder has definitions of the physical order of the layers and the relation of holes. When generating ODB++ output from your PCB design, all objects on all layers enabled for plotting will be exported.

IPC-2581

Released in March 2004, the IPC-2581[9-3] standard (titled 'Generic Requirements for Printed Board Assembly Products Manufacturing Description Data and Transfer Methodology') defines a format for integrating design data into a file to communicate from CAD to CAM machines.
IPC-2581 is similar to ODB++ in its goal of meeting the needs of both the PCB design as well as the manufacturers required information about design intent.

This format resulted from the proposal to combine the open format GenCAM and the proprietary ODB++(X) format, and it facilitates automation between CAD and CAM systems to speed up the manufacturing process. IPC-2581 is open for implementation without requiring a license, unlike ODB++. Many manufacturers support the development of IPC-2581 under the belief that an open standard will provide the greatest benefit to the industry as a whole. The establishment of a consortium in 2011 gave credibility and stability to the maturation of this format.
Understanding the IPC-2581 File Structure
The IPC-2581 format presents standards to establish a systematic process flows and to safeguard quality in a consistent and reliable manner. The IPC-2581 XML file includes:

- Copper information for etched layers
- Layer stack up information (including rigid-flex)
- Bare board netlist and in-circuit test points
- BOM
- Fabrication and assembly notes and parameters

Why You Should Use IPC-2581

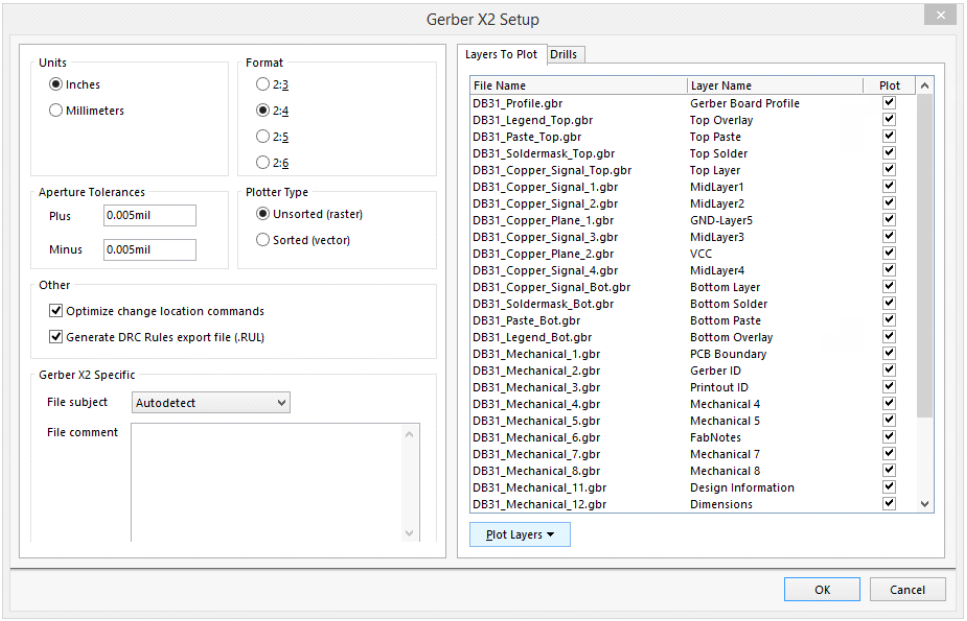
The IPC-2581 format provides similar advantages to those of ODB++ with the added convenience of being open source. The consolidated information for your design can be utilized without the supplementary files required with the Gerber format, and there is no need to convert varying files for CAM system interpretation. The danger of communicating data between CAD and CAM systems is resolved with a unified data exchange format which reduces the chance of file errors significantly.

The global adoption of IPC-2581 as an open, standardized method to consolidate transference of design data and eliminate the need for files from different formats provides a significant savings of time, finances, and resources for the industry.

The widespread adoption of the standard relies on the production and consumption throughout the industry by both designers and manufacturers, and this collaboration between EDA and supply chain companies will ultimately define the continued success of the IPC-2581 standard.

Generating IPC-2581 Files

Creating IPC-2581 files[9-11] is simple as most EDA tools will generate the files with minimal user input. Select the preferred units (Metric/Imperial) and numeric precision defined within the file to begin the export.
The precision setting determines the positional and sizing accuracy of the data within the generated IPC-2581 compliant file.



PC-2581 File Setup

Bill of Materials

At the center of every PCB design is the Bill of Materials[9-12] , which integrates all component aspects of your design to produce your finished product. The BOM is vital to the manufacturing process because it defines what, how, and where to buy every component on your board layout. In addition to component sourcing, the assembly of your final product relies on instructions found in your BOM.

A poorly documented BOM affects everyone involved in your project ranging from design, fabrication, and assembly. It is important to document as much information as possible about the physical aspects of your design including consumable items, such as glue, wires, and fasteners that are essential for the creation of your end product.

The information in your BOM should be self-encompassing and should require no further explanation to an outside party. All associated BOM records should be properly labeled to ensure all parties utilize the same BOM for design and production. Additionally, records of supporting documentation should be attached to their appropriate BOM level items.

Understanding a Bill of Materials File Structure

There are several different types of BOMs:

Modular BOM

A modular BOM describes sub-assemblies. Functionally, this BOM type operates as a database for all aspects of the sub-assemblies including parts and respective metadata. An implosion in a modular BOM associates components pieces to a major assembly while an explosion links the assembly or sub-assembly to its component.

Configurable BOM

A configurable Bill of Materials (CBOM) is a dynamic, highly versatile BOM that facilitates assembly and fabrication variants. For example, the CBOM simplifies fabrication of product lines with varying memories, such as a phone. A modular BOM structure is required to allow selection of a configured product.

Multi-Level BOMs

A Multi-level Bill of Materials, also known as a master BOM (MBOM), lists all the assemblies, components, and parts of your design. It describes the parent-children connections throughout your design represented by branches and contains all materials and components ranging from large components to glues.

Why You Should Use a Bill of Materials

The BOM conveys the structure[9-13] of your design to your manufacturer that has had no previous interactions with your design files. With a BOM in hand, your manufacturer will proceed to recreate your design in the real world with just the BOM as the guide sourcing the components, parts, and assemblies. Simply, it is an essential component of any design project.

Generating a Bill of Materials

The job of a BOM is to ensure successful construction of your final production, and you should choose a unifying specification to organize and group your components[9-14]. While you can use any specification you prefer, it is recommended to choose one that offers descriptive component types or designators.

It is also a good practice to include supplier links when possible for your components, as this will help to control pricing and availability and allow your manufacturer to easily source your parts.
When creating your Bill of Materials, be sure to include the following elements[9-15]:

- Bom level
- Part numbers
- Part type
- Part descriptions
- Quantity
- Units of measure
- Reference designators
- BOM notes

Managing Your Bill of Materials

Creating your BOM concurrently with your design helps to keep it organized, updated, and error free. Ideally, your BOM should be updated as your design is updated to reflect any changes in your component selections, pricing, and availability. Actively managing your BOM can help you to identify any sourcing, pricing, and availability issues before you hand over your documentation to manufacturing and procurement.

NC Drill Files

The Numerically Controlled (NC) drill files[9-16] contain information regarding holes/vias that are drilled through your board, and can be used to describe both plated and non-plated holes. Your design will typically have a variety of holes whether they be for through-hole parts, vias, or mounting holes. There are two types of NC drill files, a drill file and a report file.

Understanding the NC Drill File Structure

There are a number of distinct components associated with a typical NC drill file structure, including:

- Plot hole locations that tell a machine where to drill holes on your board.
- Report file that provides a synopsis of sizes and the number of drill hits to be performed.
- Associated tool numbers (drill bits) that are used to represent the individual hole sizes in your design.

Generating NC Drill Files

The generation of NC drill files[9-17] is automated in the majority of EDA tools. You will likely only need to specify the units and format to be used in your NC drill output files and the origin for your board coordinates. The formating for an NC drill file is simple with three major formating styles:

- **2:3** which has a resolution of 1 mil (1/1000 inch)
- **2:4** which has a resolution of 0.1 mil
- **2:5** which has a resolution of 0.01 mil

If you are using one of the higher resolutions, it is recommended to consult with your manufacturer about supported formats. The 2:4/2:5 formats are chosen if there are holes on a grid finer than 1 mil.

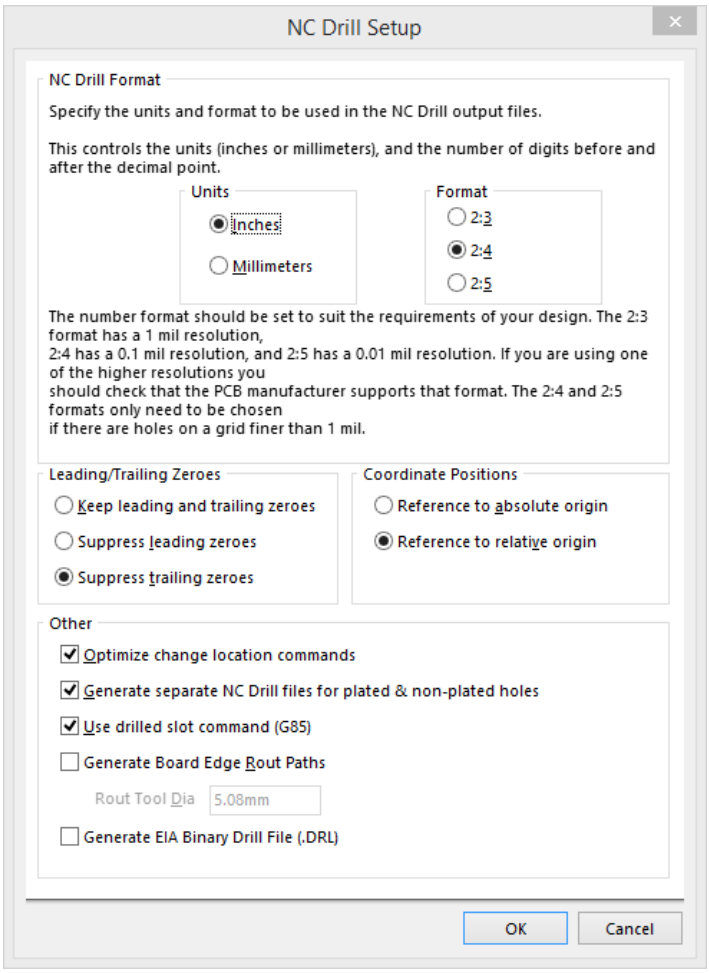


Figure 81 - NC Drill File Setup

Zero Suppression

Zero suppression reduces the file sizes by removing zeros from the start (leading) or end (trailing) of numbers.

Your NC drill files should be created with the same format and precision as your Gerber files.

> *Example: The Gerber files have been configured to use the 2:5 format, then the matching drill files should use the same format. The same would be for absolute or relative origin.*

Pick and Place Files

Pick and place machines are the standard machinery for the placement of surface mounted devices on PCB and these machines offer high speed and precision for manufacturing. Pick and place files are necessary for the proper utilization of pick and place machines.

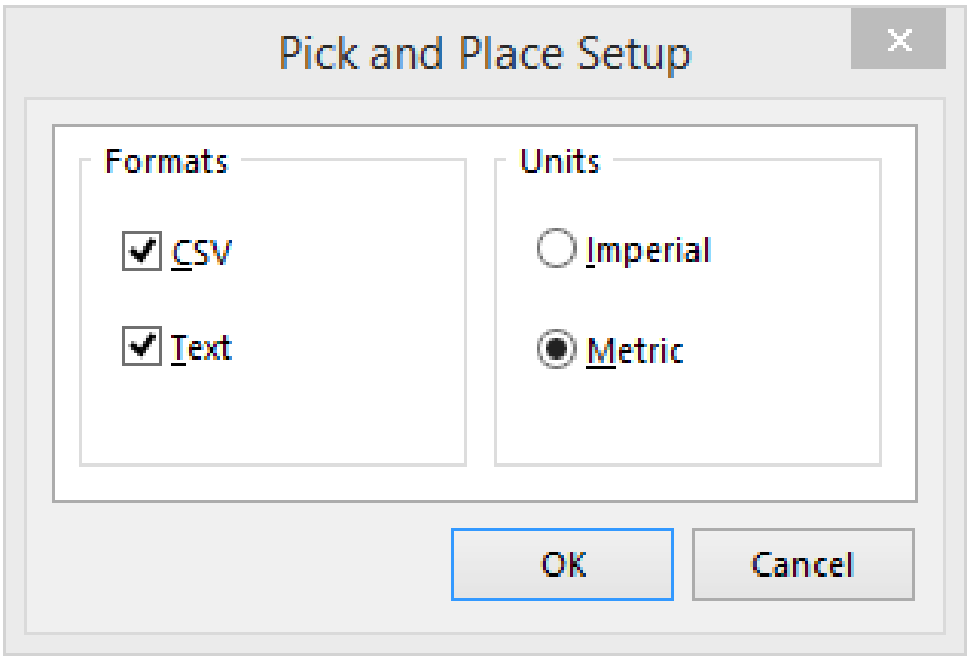
Understanding How Pick and Place Works

SMDs are fed into the pick and place machine either through tape reels or trays and are placed according to their required orientation and location then inspected with photography to identify absent and damaged components and registration errors.

Why You Should Use Pick and Place Files

With recent advancements in the manufacturing industry, the machinery used by manufacturers typically operates automatically with minimal to no human interaction. These automatic machines require precise coordinates to position components accurately according to your design documentation. Providing your manufacturer with a set of coordinates for your SMD placement simplified the automation of pick and place machinery and helps to speed up your production time at a lower overall cost.

Generating Pick and Place Files



Pick and Place File Setup

The generated files contain specific information for each component placed on your PCB[9-18]:

- Reference designator
- Footprint
- Location*
- Layer (top or bottom)
- Rotation

*Location is expressed in three ways:

- Mid X, Mid Y - component center point
- Ref X, Ref Y - component user-defined reference point
- Pad X, Pad Y - pad 1 of the component

Test Point Report Files

Once your PCB has been manufactured, in-circuit testing[9-19] (ICT) should be performed to identify sources of any shorts, opens, or other electrical issues. Typically, a bed of nails testing fixture will be implemented for these tests on large-scale productions. However, fixtureless in-circuit testing (FICT) or floating probe methods can be implemented for low complexity boards or small scale productions.

Bed of Nails Tester

The fixture[9-20] for a bed of nails tester typically takes 30 to 45 days for completion. The fixture consists of pogo pins that are positioned along test points on the PCB separated by an epoxy phenolic glass cloth laminated sheet. The pogo pins correspond to a singular test point or node of the device under test (DUT). The DUT will be held in place by a vacuum or pressed down manually by an alternate mechanism allowing the testing of all points concurrently.
Figure 83 shows an example setup for a bed of nails tester.

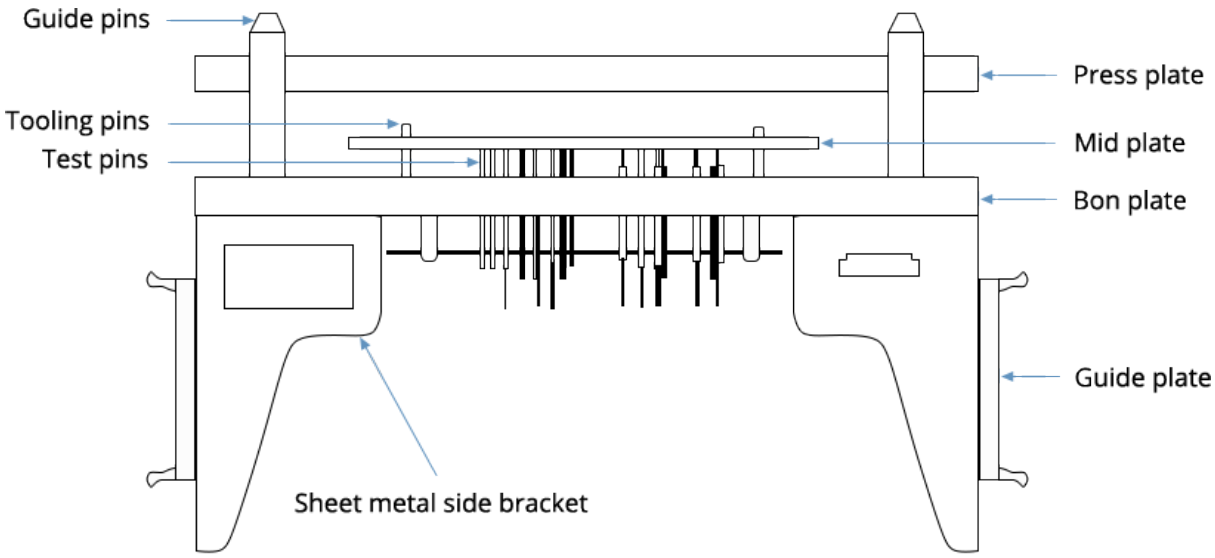


Figure 83 - Bed of Nails Tester

Fixtureless In-circuit Test

A fixtureless in-circuit test is a great alternative for smaller volume productions, and this method allows you to skip the construction of a physical fixture. All component inspection and test probe positions are computer operated, and the removal of physical wires and pins reduces the capacitive strain on your PCB and provides more accurate measurements.

Floating Probe

A floating probe measures voltage potential across two non-ground potential points. These measurements can prove a challenge for fast AC signals as measurement quality can only be assured with confinement from the ground potential of the DUT. If this confinement is not met, it is impossible to have consistent and accurate measurements. You will commonly find this measurement system being used for power circuitry testing.

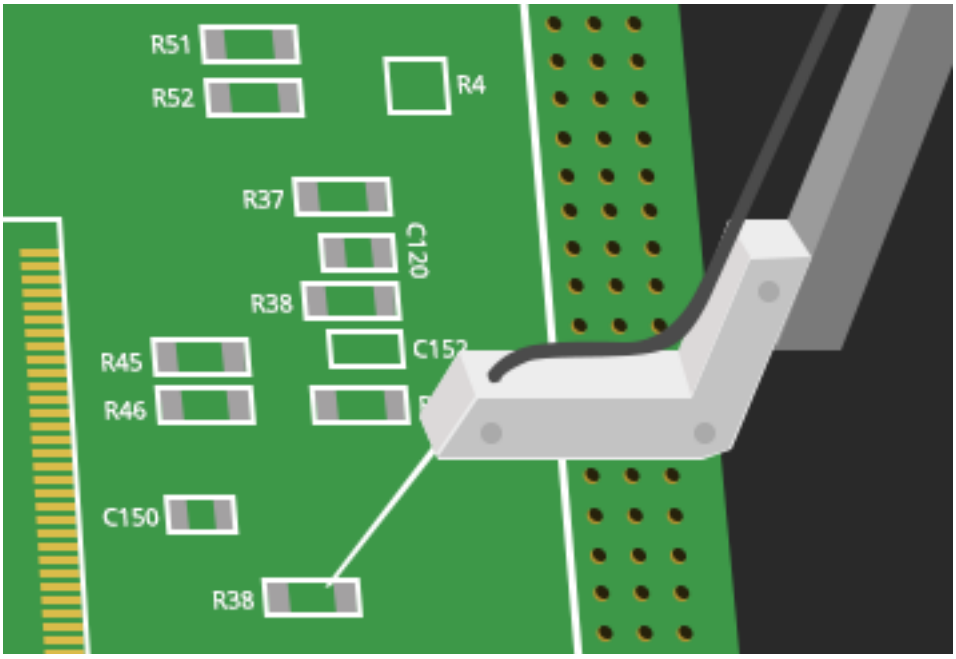
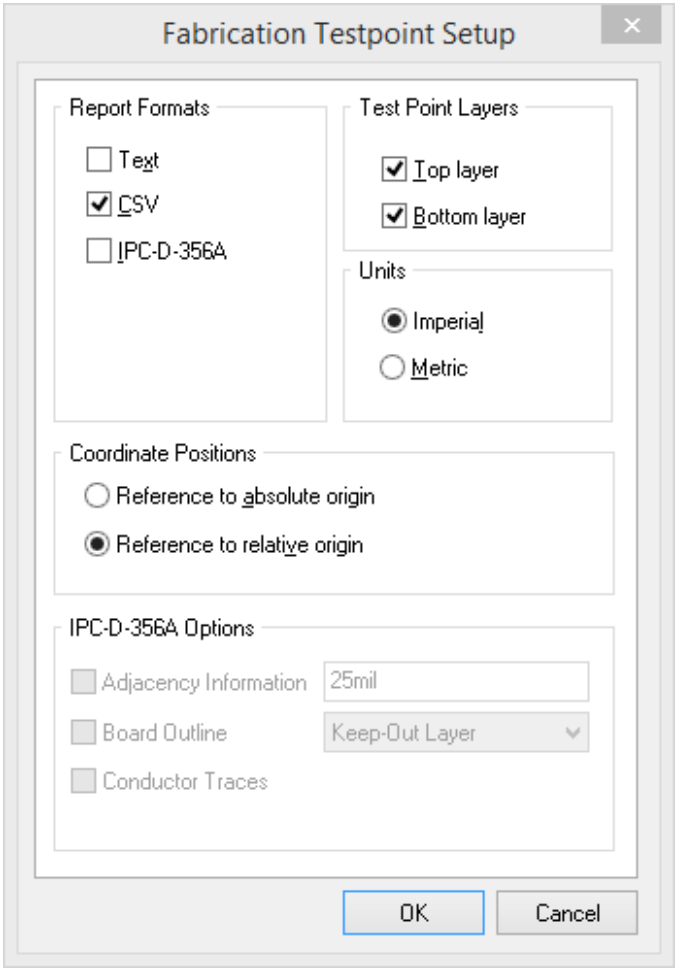


Figure 84 - Floating Probe

Generating Test Point Report Files



Test Point Report File Setup

It is recommended to generate separate testpoint reports[9-21] for fabrication and assembly, with the format being in either text, CSV, or IPC-D-356 format. Test point locations will have been decided in your design process, being on either the top, bottom, or both layers of your board.

Netlists

The purpose of the netlist[9-22] is to describe the electronic circuit connectivity of your design and is comprised of lists of related electronic circuitry. The list contains information on pins and the connected circuitry (instances), which is commonly referred to as nets. Although the composition and intricate circuitry definitions differ, all netlists boil down to lists of nets and their connected circuitry.

Understanding the Netlist File Structure

In a netlist, an instance refers to contained or referenced descriptions of parts used within your design. If a pin connects to several other pins, the netlist will create unique names to differentiate between the connections even if they stem from the same pin.

Why You Should Use Netlists

Netlists[9-23] play an important role in physical verification of your board. A layout versus schematic (LVS) verification protects your product from incorrect physical component placement, and the LVS verification safeguards quality manufacturing processes, like solder bridging. Netlists also facilitate post layout simulation and allow for testing of parasitic circuits. This post layout simulation process checks for any discrepancies in circuitry performance to eliminate errors in production.

IPC-D-356 Files

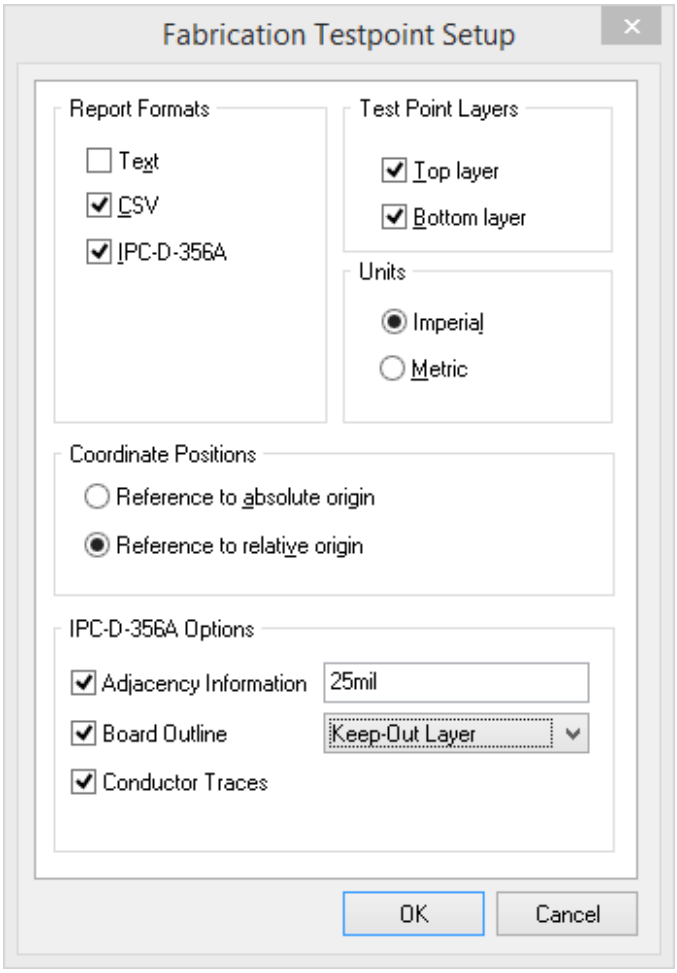
An IPC-D-356[9-24] file is a netlist used for test point reports and is a highly recommended standard for developing test point fixtures and program definitions for your design. This format is simple to document test point descriptions and positions with the added benefit of the inclusion of net names and pin/reference designators.

Understanding the IPC-D-356 File Structure

The IPC-D-356 format can be viewed as a specialized netlist for test points that couples board coordinates with net names, reference designators, and pin/pad details. IPC-D-356 files are formatted into ASCII columns with the initial three characters designating the test point type. This information is followed by netnames, reference designators, and pin information or pad sizes. Unifying this test information into a single format increases regularity and positive board yields.

Generating IPC-D-356 Files

Refer to the section on test point report generation for more information about general setup requirements. When you are using IPC-D-356[9-25], you should provide adjacency information for a list of nets that could be shorted. The adjacency is based on a minimum feature clearance. Net adjacency is used to reduce isolation testing on flying probe test systems and other test coverage.



IPC-D-356 File Setup

Finalizing Your Manufacturing Files

Building a list of manufacturing files is a final critical step of every PCB design process, and these files are often your first and only method for successfully communicating design intent to your manufacturer. Between clarifying board layer composition in an ODB++, IPC-2581, or Gerber file to specify part sourcing in a BOM, every data-rich file that you add to your completed design goes lengths towards ensuring the manufacturability of your board.

Conclusion

Design for Manufacturability isn't just about your design process, it is about being aware of what happens both before and after you complete your board layout, from the first component you place digitally to the last part a pick-and-place machine places physically on your PCB. At its core, DFM is as much an art as it is a science, requiring engineers to be aware not only of their own cares and concerns in the design process but every stakeholder's needs as well. If there is one thing we can say for certain in the world of electronics design, it is that no one part of this process exists in isolation, and everything is connected.

Every decision that you make as a PCB designer has a reaching effect down the road, from how your board is manufactured to a facility to the end product delivered to your customers. And when you're designing for manufacturability, you're designing for trust, reliability, and integrity in each and every product that you create.

While this guidebook is extensive in scope, it is just the tip of the iceberg for your journey into the world of DFM. Standards will continue to change, processes will continue to be refined, and manufacturing will continue to get more efficient, but the fundamentals will remain the same. To design a successful PCB right the first time, you need to look through a wider lens and see the design you produce in the digital domain as one small piece of a greater puzzle. Shipping off your design and documentation to manufacturing isn't the end, but merely the beginning of a much larger ecosystem.

Having reached the end of this guidebook, you should have a new, well-rounded perspective on which to base your future design decisions. The first section looked at intricacies of the typical PCB design process and outlined specific guidelines to help you create manufacturable boards better, faster, and more reliable than ever. This process has many overarching elements, from the materials you select for your layers, to strategizing the placement of your components and test points.

From there, you moved beyond the design process to documentation, exploring what makes up a complete set of documentation required by every manufacturer. It started with the basic components of a PCB template, and then dived into the finer details, covering how to assemble your master drawing and prepare your manufacturing files.

Regardless of where your interests lead you after completing this guidebook, it is our hope that you've walked away with a clearer understanding of how to accomplish the goals that were set out at the beginning:

- Eliminate the need for multiple board respins due to manufacturing-specific details that were missed in a design process.
- Design and produce boards that are both manufacturable and function as intended by following a set of best practices set forth by industry-leading manufacturers.
- Reduce the time spent on design revisions and ultimately meet time to market goals consistently by following a set of design practices for board layout and documentation.

And the most important goal of all - **getting a good board back from manufacturing right the first time, every time.**

Glossary

BALL GRID ARRAY (BGA) - The ball grid array is package for integrated circuits. Instead of leads, it has a grid of pads to which are attached balls made from solder. The IC die inside the package has metallized terminations for interconnecting to the solder balls. BGA packages offer much greater connection density than packages with pins on the perimeter. The case type number of a chip component indicates its size. For example: a 1206 chip is 0.120" long by 0.060" wide, and a 1812 chip is 0.180" long by 0.120" wide.
ANNULAR RINGS - The conductive material on the pad that surrounds the hole, which is difference between the pad diameter and the corresponding drill diameter.
APERTURES - A defined space shape in a Gerber file used to create images of your layers.
ARC - Utilize the current aperture to create circular segments and always has rounded endings for Gerber files.
ASPECT RATIO - The ratio between the thickness of the board and the size of the drilled hole before plating.
AUTO PLACEMENT INSERTION - A technology that automates the stuffing and populating PCB with all type of IC packages.
BARE BOARD - An unpopulated or unstuffed PCB without components.
BLIND VIA - A via which connects an outer layer to one or more inner layers but not to the other outer layers.
BOW & TWIST - A Printed Circuit Board characteristics that determine its flatness, flexibility, and durability. Bow and twist requirements are usually noted on the master drawing.
BURIED VIA - A via which connects one or more inner layers, but not to an outer layer.
CAPTIVE PRESS-FIT STUDS - Threaded self-clinching studs designed for quick PCB installation using a simple press.
COEFFICIENT OF THERMAL EXPANSION (CTE) - Measures the fractional change in size of an object relative to the change in temperature. It is generally expressed as the

change in size per degree with constant pressure.

COLD SOLDER JOINTS - Unreliable and poor soldering areas where the solder did not melt completely. The solder joint will be weak and may break overtime. A cold solder joint may also be resistive and cause functional problems.

CONDUCTOR - An electrical path between two component pads.
Also referred to as a “trace”, “path”, or “line”.

CONFORMAL COATING - A thin protective chemical coating that conforms to the topology of the PCB, protecting the circuitry.

DATUMS - A reference point located on the printed board, usually a hole, that allows a machine to “see” how the board is oriented in space.

DECOUPLING CAPACITORS - Also known as bypass capacitors, are used to suppress the high-frequency noise in power supply signals, and can act as tiny power supplies when the main power supply temporarily drops its voltage.

DESIGN FOR MANUFACTURING (DFM) - The process of designing a functional and reliable PCB that is easy to manufacture.

DIELECTRIC CONSTANT - The ratio of the permittivity of a substance to the permittivity of free space.

DRAW OBJECTS - Produce a straight line with thickness and endings dependent on the shape of the current aperture.

DRILL DRAWING TABLE - Lists the size and number of holes for each drill used on the board. Each drill size can be represented by a symbol, a letter or the actual hole size.

ELECTRO-DEPOSITED (ED) COPPER - A type of copper used to produce rigid PCBs. ED copper has the advantage of obtaining tight etched spacing and well defined conductor walls. It also has a rougher surface, than rolled copper, which benefits bonding strength.

ELECTROLESS COPPER - A widely used technique of depositing copper chemically to form plated-through holes.

ELECTROSTATIC DISCHARGE (ESD) - The sudden flow of electricity between two electrically charged objects caused by contact, an electrical short, or dielectric breakdown. Every PCB requires ESD testing and certification.

EPOXIED CHIP - Epoxy is usually applied to ICs with very thin wires to give them stronger mechanical bonding. It can also be applied to the bottom layer to secure components in place, during wave soldering, on a double-sided board that uses mixed technologies (SMT and through-hole).

ETCHBACK - Chemical etching of plated through holes. There are two possible processes, positive etchback and negative etchback. The less expensive negative etchback results in the land around the hole being slightly recessed from the hole. Positive etchback is used in high-reliability applications and etches the hole itself so that the land very slightly overlaps the hole.

EXTENDED CODE COMMANDS - Two letter codes paired with the “%” sign for Gerber files.

EYELETS - A hollow conductive tube that is used to create electrical connections from

one side of a board to another or/also as physical support.

FIDUCIAL MARK - A round pad or other mark on the surface of a PWB used for optically aligning automatic insertion equipment to the component footprints on the board.

FLASHES - Reproduction of apertures than are often reproduced many times and are commonly used to create pads for Gerber files.

FR-4 - A flame retardant woven glass fabric with epoxy resin, primarily used in the production of Printed Circuit Boards.

FUNCTION CODE COMMANDS - Single letter codes beginning with D/G/M and a positive integer for Gerber files.

GLASS TRANSITION TEMPERATURE (Tg) - The temperature region at which epoxy (Polymer) reverses its states (transitions) from a hard glassy material, to a soft, molten, rubbery material.

HYBRID PCB - Mixed component technology, with both surface mount components and through-hole components.

IN-CIRCUIT TEST (ICT) - A powerful test technique that uses a bed of nails, or flying probes, to gain access to all the nodes of a populated PCB, to test it for shorts, opens, capacitance, resistance, and other performance tests. Software is usually written for each board type to instruct the system what tests to perform.

LAMINATE - A dielectric material, usually infused with glass, upon which the conductive material is attached.The material can be either flexible or riged.

LAMINATION - The process of achieving improved material strength and stability by bonding (pressing) together two or more layers of material.

LAND - A land is the remaining conductive material that remains after etching. It is used for attachment or connection of components and for conduction of signals across the PCB. See also “Pad” and “Trace”.

LAND PATTERN (“LANDS” OR “PADS”) - A combination of lands intended for the mounting and interconnection of a particular component.

NC (Numerical Control) Drill File - A PCB fabrication file that defines the tools, locations (X & Y coordinates), and hole sizes that are to be drilled

PAD - A pad is the remaining conductive material after etching. Pads are a common part of component footprints and can be surface mount or through hole. A pad is the connection point where the copper on the PCB and leads on the component connect. See also “Land” and “Trace”.

PANELIZATION - The method of placing two or more PCBs onto one panel, which allows multiple boards to be made at the same time, reducing cost. It also allows boards to be secured during manufacturing, shipping, and assembly.

PART NUMBER - A unique number used to identify a part design within a corporation for consistent and easy reference.

PLANES - Planes are special solid copper internal layers, typically used to provide an electrically stable ground or power reference throughout the PCB.

PLASTIC LEADED CHIP CARRIER (PLCC) - A square component package commonly

having J-leads on all four sides.

POLARITY INDICATORS - Indicate components that can be connected to a circuit only in one direction (e.g. polarized capacitors, diodes, & LEDs). Additionally, the intent of the indicator is to match the alignment mark on the component, but not necessarily interpret the polarity.

PREPREG - An abbreviation of pre-impregnated, which is fiberglass impregnated with a resin bonding agent.

PTH (PLATED THROUGH HOLE) - A hole in which electrical connection is made between external or internal layers or both, by the plating of metal on the wall of the hole. Also used for mounting the leads of through hole components.

REFERENCE DESIGNATOR - Reference designators identify components on a electrical schematic or on a Printed Circuit Board. The reference designator usually consists of one or two letters followed by a number, e.g. R23, TP12.

REFLOW SOLDERING - A process of soldering surface mount components to a PCB by mass heating of the entire assembly. The heating process causes solder paste, pre-applied to component land patterns, to melt and form solder fillets between the component leads and land patterns on the board. The heating may be done with infrared radiation or by heating a liquid to its boiling point (the vapor phase change) to transfer heat to the solder. Both are generally done in an inert gas atmosphere.

REGIONS - Sections defined by linear and circular segments and are commonly used for copper pours for Gerber files.

REGISTRATION - The process of aligning layers of a PCB with holes that have been precisely drilled in specific locations.

RESIN - A high-temperature thermoplastic used with glass to manufacture multilayered printed circuit laminates.

RESISTOR PACK - Resistors that come in pre-wired packs. Sometimes the resistor pack array shares a common pin.

RESTRICTION OF HAZARDOUS SUBSTANCES (RoHS) - A European directive, though widely adopted worldwide, that aims to reduce the use of hazardous substances in electrical and electronics equipment. It also requires heavy metals such as lead, mercury, cadmium, and hexavalent chromium and flame retardants such as polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE) to be replaced by safer alternatives.

ROLLED COPPER - A type of copper, made very thin by processing between heavy rollers, extensively used to produce flexible PCBs. Its smooth surface makes it ideal for flexible applications.

SHADOWING - The blocking of the solder wave from small components by larger components or through hole component pins.

SIP-TYPE PACKAGES - IC Packages that have one row of connecting pins (e.g. memory module).

SMALL OUTLINE TRANSISTORS (SOT) - A discrete semiconductor package having two

gull wing leads on one side and one on the other side.

SOLDER BRIDGING - The merging of two solder joints that form an unintended connection between the two.

SOLDER FILLET - A general term used to describe the contour of the solder joints formed between the component termination and the PWB land pattern after soldering.

SOLDERMASK - A coating of material used to protect or mask conductive traces or areas of a PWB against solder bridging.

SOLDER PASTE - A combination of minute spherical solder particles, flux, solvent and a suspension agent which is used in reflow soldering. Solder paste is deposited onto the substrate by solder dispensing and screen or stencil printing.

SOLDER PLUG -

SOLDER SIDE (BOTTOM) - A term used to describe the soldered side of a PWB using through hole technology.

SURFACE MOUNT DEVICE (SMD) - A device that is not inserted into through holes, but designed for placement and soldering onto pads on the surface of a substrate.

SURFACE MOUNT TECHNOLOGY (SMT) - The technology of assembling PCBs and hybrid circuits where components are mounted onto pads on the surface of the substrate rather than into through holes.

SMALL OUTLINE INTEGRATED CIRCUIT – (SOIC) - An integrated circuit package having two parallel rows of gull wing leads. Packages currently range from 8 to 40 leads.

TEARDROP PADS - Added copper/metal to a pad in order to reduce the mechanical and thermal stresses, and to create a stronger track-to pad, track-to-via and track-to-track connections.

TEST POINT - A via or a pad with its own reference designator for probing and testing the nodes on a PCB.

THERMAL RELIEF - A technique used with vias and holes to maintain process temperature to prevent poor hole filling and cold solder joints, as the copper in a multilayer board can turn into a heat sink.

TOMBSTONE (DRAWBRIDGE) - The condition which exists when a defect in soldering, component orientation, component type or other factors have caused one end of a chip component to pull off the solder pad resulting in a open circuit. The component may stand on end in a vertical or near vertical position.

TOOLING HOLES - A general term used for holes or slots in PWBs or blank material to aid in the manufacturing process.

TRACE - A conductive path or line. See also “Land” and “Pad”.

VIA - A plated through hole used as a through connection for conductors from the component side to solder side of the board or an outer layer to an inner layer. A via is not intended for mounting components.

WAVE SOLDER -The soldering of an assembly by passing the surface mount components, mounted on the solder side of the board, over an adhesive and then over a molten wave of solder. Typically through hole components installed on the top side of the board are soldered at the same time. The application of solder paste is not required for this assembly.

ZIF SOCKETS - A zero-insertion-force socket for mounting electronic devices that is designed not to stress or damage them during insertion.

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Appendix A - Gerber File Command Codes

Command Code	Definition
D01	When region mode is off, used to create draw and arc objects. When region mode is on, used to create linear and circular segments.
D02	Moves current point to coordinate.
D03	When region mode is off, flashes the current aperture. Command is not allowed when region mode is off.
Dxy*	Sets the current aperture to xx defined by AD command. *(xy can be defined as any number greater than nine as D01-D09 are reserved).
G01	Executes a D01 code operation to produce a draw from current point to specified coordinates.
G02	Executes a D01 code operation to produce an arc from current point to specified coordinates and offset in clockwise orientation from start to end point.
G03	Executes a D01 code operation to produce an arc from current point to specified coordinates and offset in counterclockwise orientation from start to end point.
G04	Used for comments.
G36	Enable region mode.
G37	Disable region mode.
G74	Limits arc creation to 90° from starting point. Each quadrant will require its own operation.
G75	Allows creation of full 360° arcs with a full circle being defined as 360°.
M02	End of file marker.
FS	A mandatory command used to define coordinate number format at beginning of file. Format defines integer lengths and decimal precision.
MO	A mandatory command used to define the units of coordinates, parameters, and modifiers.

AD	Sets aperture definition to a designated D code number.
AM	Defines macro apertures which can be referenced from the AD command.
SR	Creates a block containing a set comprised of a command stream to execute recursively for creating graphic objects.
LP*	Creates a level and sets its initial polarity. * Followed by C for clear polarity (LPC) and D for dark polarity (LPD).